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The timing system on the J-TEXT tokamak

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HIGHLIGHTS

- The timing system achieved tree structured timing network with only one type of timing module.
- This system is integrated into J-TEXT COADC which is an EPICS based control system.
- This system handles multiple timing sequences and events.
- This system has been deployed on J-TEXT and working properly in daily experiments.

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ABSTRACT

This paper describes the timing system designed to control the operation time-sequence and to generate clocks for various sub-systems on J-TEXT tokamak. The J-TEXT timing system is organized as a distributed system which is connected by a tree-structured optical fiber network. It can generate delayed triggers and gate signals (0 μs–4000 s), while providing reference clocks for other sub-systems. Besides, it provides event handling and timestamping functions. It is integrated into the J-TEXT Control, Data Access and Communication (J-TEXT CODAC) system, and it can be monitored and configured by Experimental Physics and Industrial Control System (EPICS). The configuration of this system including tree-structured network is managed in XML files by dedicated management software. This system has already been deployed on J-TEXT tokamak and it is serving J-TEXT in daily experiments.

1. Introduction

The J-TEXT (Joint Texas Experimental Tokamak, formerly TEXT-U) facility is an experimental platform for magnetic confinement fusion research [1]. The plasma in J-TEXT tokamak lasts for about 300 ms. J-TEXT is equipped with more than 15 kinds of diagnostic systems, and has more than 700 data acquisition channels. During an operation cycle, various sub-systems need to be triggered at a preset sequence, and reference clocks should be distributed to the data acquisition system and the real-time plasma control system, therefor timing system is needed. As the J-TEXT experiments get more complicated, event handling is also a required function of the timing system.

J-TEXT is currently undergoing a major control system upgrade. New controllers at J-TEXT based on PXI/PXIe hardware will be equipped with an IEEE-1588 adaptor and support the Precision Time Protocol (PTP) for time synchronization and events generating [2]. But before the new controllers are fully deployed, the old controllers which require TTL clocks and triggers are still the workhorses. A timing system is needed to bridge the gap between the inadequate old software central trigger system [3] and the IEEE-1588 PTP. Different research facilities have different approaches for timing system. One popular approach is a star-shaped network with VME card based timing modules; the central timing module distributes clocks and encoded events, and the local timing module decode and output the events, generate delayed triggers or clocks [4,5]. There are also tree-structured designs that rely on relay modules [6–8]. Inspired by the EAST synchronization and timing system [9], the J-TEXT timing system composed by stand-alone units based on Field-Programmable Gate Array (FPGA) has been developed. Unlike existing systems, the J-TEXT timing system achieved tree-structured network with only one type of module, thus there is no

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central module or relay modules. Moreover, each module can be programmed with multiple timing sequences, and these sequences can be executed according to external events. Each output channel of the timing module can be configured to provide clock, trigger pulse and gate signal.

The timing system is designed to be integrated into the J-TEXT Control, Data Access and Communication (J-TEXT CODAC) System, which is a scaled down version of ITER Instrumentation and Control System. All the status and functions of the timing system can be monitored and configured using Experimental Physics and Industrial Control System (EPICS) [10] software. Besides, dedicated management software is provided, which not only programs the operation sequence, but also manages the tree-structured network of the system.

2. System design

2.1. Requirements of the timing system

The old software based trigger system of J-TEXT can only provide triggers with 1 ms time resolution, no clock nor gate signal is available. It has only one trigger module shared by the whole J-TEXT site. To replace the old trigger system, the timing system should be a distributed flexible system with tree-structured network. It will be able to deliver triggers, clocks, and gate signals at 1 μs time resolution with duration of 4000 s. The ability of outputting multiple timing sequences based on trigger events and timestamping these events is required. It also needs to be integrated into the newly deployed J-TEXT CODAC system. Last but not least, the costs of this system must be low.

2.2. Structure design

According to ITER CODAC design principle, a set of instruments and controllers that belong to the same sub-system and are responsible for the same technical function is called a plant-system (PS) [11]. The timing system will have distributed timing modules serving different PSs connected by tree-structured network. Each tree node is a module which can generate trigger, gate and reference clock signals, so it is called a Timing Node (TN). Each TN receives trigger and clock from its parent TN.

The timing system is integrated into the J-TEXT CODAC system. All the controllers in PSs are controlled and monitored by Central CODAC system (CCS) to achieve integrated control. The CCS communicates with controllers in PSs with EPCIS Channel Access (CA) protocol via Plant Operate Network (PON). To be integrated into J-TEXT CODAC system, the TNs in the timing system have to support EPICS and be connected to the PON. Fig. 1 is a simplified block diagram of the control system of a PS. The Plant System Host (PSH) in each PS provides communication between J-TEXT CCS and the custom-built devices which do not support EPICS. It also monitors controllers inside the PS and synthesizes PS status. TNs are connected to the PSH as custom-built devices. The PSH publishes the status and configurations of the TN as a series of EPICS Process Variables (PV) on the PON as well as dispatches the commands from the CCS to the TN.

Fig. 2 shows the system topology, the configuration and monitor of the timing system are centralized in the CCS. The trigger and clock outputs of a TN are carried by the timing network which is a tree-structured network connected by optical fiber. All the triggers and clocks can be consumed either by instruments and controllers in a PS or by child TNs. All the nodes in this tree-structured network are identical, thus, no central nor relay node is required. Parent and child TNs are connected by a pair of optical fiber; one TN can be a parent and child node simultaneously, thus the timing network can be very flexible. The timing system also comes with management software, which not only programs the experiment sequence but also configures the tree-structured timing network.

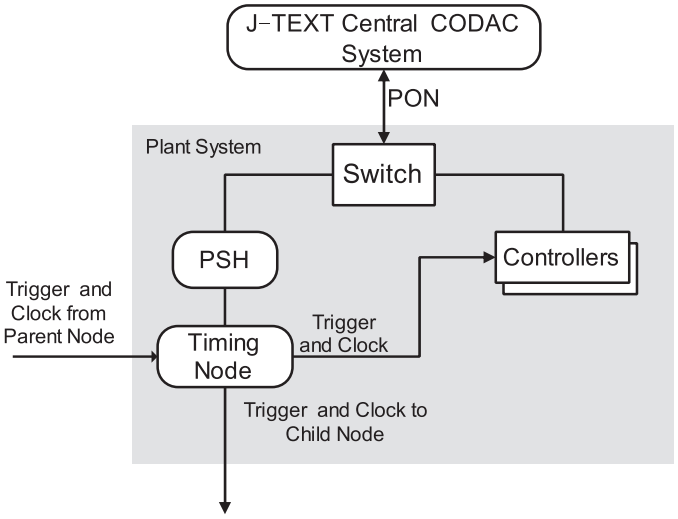

Fig. 1. The integration of the timing system; the grey part represents the control system of a PS.

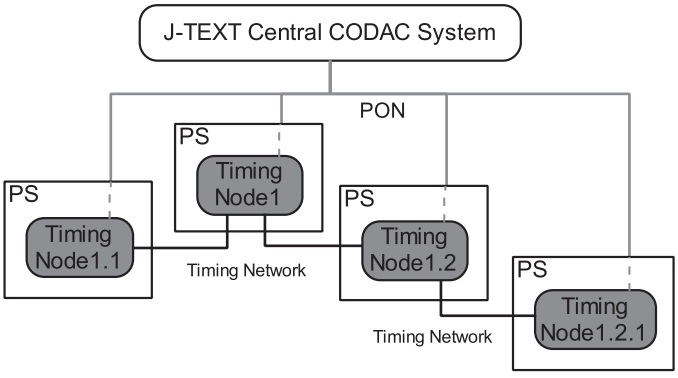

Fig. 2. The topology of the timing system, the grey lines stand for the PON, the black lines stand for the timing network. In this figure TN1 is the root node, TN1.1 and TN1.2 are the children of TN1, TN1.2.1 is the child of TN1.2.

3. Implementation

This section will present the implementation of the timing system, including the implementation of the TN hardware, the PSH configuration for the TN, and the management software.

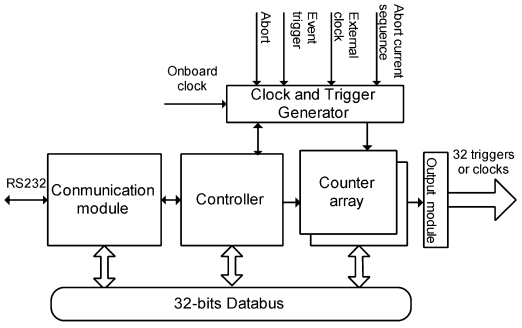

Fig. 3. The FPGA core top design block diagram.