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Data reduction in the ITMS system through a data acquisition model with self-adaptive sampling rate

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Abstract

Long pulse or steady state operation of fusion experiments require data acquisition and processing systems that reduce the volume of data involved. The availability of self-adaptive sampling rate systems and the use of real-time lossless data compression techniques can help solve these problems. The former is important for continuous adaptation of sampling frequency for experimental requirements. The latter allows the maintenance of continuous digitization under limited memory conditions. This can be achieved by permanent transmission of compressed data to other systems. The compacted transfer ensures the use of minimum bandwidth. This paper presents an implementation based on intelligent test and measurement system (ITMS), a data acquisition system architecture with multiprocessing capabilities that permits it to adapt the system's sampling frequency throughout the experiment. The sampling rate can be controlled depending on the experiment's specific requirements by using an external dc voltage signal or by defining user events through software. The system takes advantage of the high processing capabilities of the ITMS platform to implement a data reduction mechanism based in lossless data compression algorithms which are themselves based in periodic deltas.

Keywords: Real-time data acquisition and processing; Adaptive sampling; Lossless compression; Advanced intelligent instrumentation

1. Introduction

One goal in data acquisition systems used in long pulse or steady state fusion diagnostics is to acquire capabilities to adapt the sampling rate depending on the experiment's time evolution. Another is to compress the acquired information in order to reduce the high amount of data to be processed, and therefore reduce the required network bandwidth and storage requirements. In order to achieve these goals, flexible data acquisition system architecture that can be easily customized to specific experiment requirements within a short development time is needed [1,2]. The ITMS platform is an example of such system architecture. The final goal of ITMS is to offer a technology, consisting of a set of hardware and software tools that allows the development of advanced intelligent instruments (AII) with fast data acquisition and processing capabilities that can be reconfigured through software. The system architecture and the use of fourth generation programming languages, such as LabVIEW, allow the reduction of development time substantially.

This paper presents an application of this technology to implement a data acquisition and processing system that has adaptive sampling capabilities, and can also compress the acquired data before sending it to a database server or to other processing systems through a network connection. Both features reduce the amount of data acquired by the system, while maintaining the same amount of information, allowing a reduction of the required transmission bandwidth and storage requirements of the overall system. Adaptive sampling capabilities means that the sampling rate of data acquisition cards that are used can be changed dynamically, e.g. during the experiment duration, according to specific requirements. In order to keep track of the sampling frequency used to acquire each sample,

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this system uses an analogue dc voltage applied to an input of each data acquisition card, which is related to the sampling rate being used. There is a direct relation between the dc voltage value of that input channel and the sampling frequency being used to acquire the rest of the channels (see Section 3). The system also includes a data reduction mechanism that is implemented based in data compression algorithms developed in LabVIEW [3].

2. ITMS architecture

Fig. 1 shows the hardware architecture of the ITMS platform adapted to this application. The hardware consists of the following elements:

- One standard PXI chassis, with an embedded system CPU (SCPU). SCPU is used to configure data acquisition cards (DAQ), to acquire data from DAQ channels, to distribute the acquired data among system's CPUs and to process the data of desired channels.
- Several DAQ cards.
- Several peripheral CPU cards (PCPU) allocated in peripheral PXI slots (CC8-BLUES Pentium 3 from EKF System or Inova ICP-PM-4). PCPUs are used to process the data acquired from desired channels. PCPUs will increase the computing capacity of the PXI platform as compared to typical PXI systems based only in the system CPU controller [2].

ITMS software architecture is based in three software modules that run both in the SCPU and in the PCPUs (Fig. 2): Setup&DAQ, dynamic data processing system (DDPS) and event detection and sample rate modification (EDSRM). These modules were developed using Linux kernel modules (Fedora Core 1) based on RTAI (Version 3.3), the COMEDI data acquisition driver and LabVIEW (Version 8.2).

The Setup&DAQ module deals with the data acquisition and distribution configuration and the acquisition and data distribution among processing elements of the system (PCPUs and SCPU). The user interface was developed in LabVIEW, while the data acquisition and distribution part was coded using Linux kernel modules. The part that deals with the continuous data collection in the final user applications was developed in C and integrated in LabVIEW code by using code interface nodes (CINs).

The DDPS module is in charge of running the data processing routines defined by the user. These routines were developed in LabVIEW. The results obtained by DDPS are sent to another computer using the network connection.

The EDSRM module is a client-server application that runs in each CPU (SCPU or PCPUs). The client, which usually runs in the PCPUs, detects the events generated by the DDPS module and sends them to the server module as messages through TCP/IP. The server, which always runs in the SCPU, receives the messages from the clients, or any other external systems, and updates the sampling rate accordingly. Sampling rate changes can also be caused by external systems by applying an external dc voltage signal to one of the system's inputs (external sampling rate control signal). The relation between the sampling frequency and the external dc voltage value is defined during the system configuration process. The EDSRM server also checks for changes in this voltage to detect sampling rate modification requests.

3. Implementation of the adaptive sampling rate model in the ITMS

Sampling rate in commercial data acquisition cards is controlled through an internal or external clock signal. The raw data acquired from the card does not include any information about the sampling rate that has been used to acquire it. The sampling rate information is added by the data acquisition driver when it collects the data, according to the data acquisition configuration information. Fig. 3 shows how the ITMS hardware architecture was modified to implement adaptive sampling rate. The DAQ's external clock input is used to control the acquisition process. This clock is generated using a counter of an additional DAQ card (DAQ0), whose input can be chosen between an external master clock signal connected to the clock's source input, or the internal DAQ timebase clock. In addition, one analog input channel of the DAQ card is used to read the value of the external sampling rate control signal. Finally, an analog output voltage channel of the same card is used to generate the mark voltage

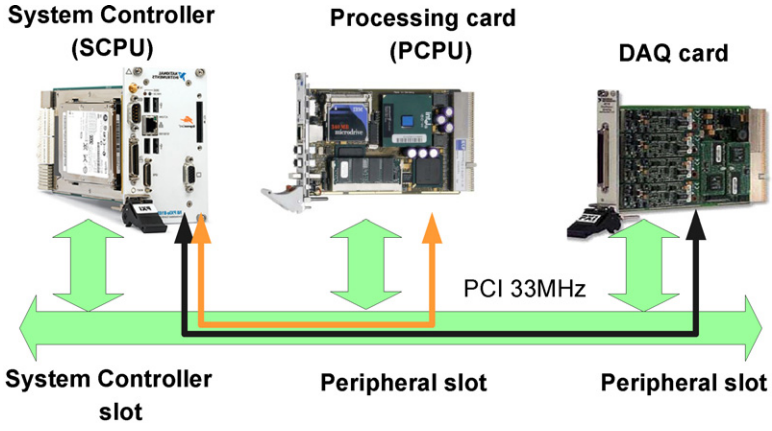

Fig. 1. Standard ITMS platform hardware architecture.