NDT&E International 79 (2016) 1–6

Contents lists available at ScienceDirect

NDT&E International

journal homepage: www.elsevier.com/locate/ndteint

Characterization of micro-crack propagation through analysis of edge effect in acoustic microimaging of microelectronic packages

Chean Shen Lee [a], Guang-Ming Zhang [a,*], David M. Harvey [a], Ailing Qi [b]

[a] General Engineering Research Institute, Liverpool John Moores University, Byrom Street, L3 3AF, United Kingdom
[b] School of Computer Science and Technology, Xi'an University of Science and Technology, Xi'an 710054, China

ARTICLE INFO

Article history:
Received 27 July 2015
Received in revised form
5 November 2015
Accepted 8 November 2015
Available online 3 December 2015

Keywords:
Crack propagation
Acoustic microimaging
Microelectronic package
Edge effect
Accelerated thermal cycling

ABSTRACT

The miniaturization and three dimensional die stacking in advanced microelectronic packages poses a big challenge to their non-destructive evaluation by acoustic microimaging. In particular, their complicated structures and multiple interfaces make the interpretation of acoustic data even more difficult. A common phenomenon observed in acoustic microimaging of microelectronic packages is the edge effect phenomena, which obscures the detection of defects such as cracks and voids.

In this paper, two dimensional finite element modelling is firstly carried out to numerically simulate acoustic microimaging of modern microelectronic packages. A flip-chip with a 140 μm solder bump and a 230 MHz virtual transducer with a spot size of 16 μm are modelled. Crack propagation in the solder bump is further modelled, and B-scan images for different sizes of micro-cracks are obtained. C-line plots are then derived from the simulated B-scan images to quantitatively analyze the edge effect. Gradual progression of the crack is found to have a predictable influence on the edge effect profile. By exploiting this feature, a crack propagation characterization method is developed. Finally, an experiment based on the accelerated thermal cycling test is designed to verify the proposed method.

1. Introduction

With the miniaturization of electronic devices, the solder bump pitches are increasingly dense with diameters as small as 30 μm and decreasing. Moreover, many electronic devices are used in hostile environments. For example, in automobiles, electronic control units deal with vast temperature differences and constant vibrations. This brings into question the structural reliability of such devices [1]. According to Wunderle [2], up 65% of failures are thermo-mechanically related. Accelerated environment testing offers a way to evaluate the lifetime of such devices [3]. During thermal cycling, a crack will initiate in the solder bump and propagate through the solder bump structure, eventually resulting in an electrical discontinuity. It is observed that this particular failure mode usually occurs close to the silicon die to bump interface for the flip chip packages. To determine the crack size quantitatively in between thermally cycles, destructive evaluation on the sample often has to use in industry where a cross-section will be cut, polished and optically examined.

Acoustic microimaging (AMI) is effective at detecting discontinuities inside a test sample, which makes it ideal of non-destructive evaluation of solder bump discontinuities [4–7]. Edge effect [8] is a physical phenomenon in acoustic imaging of microelectronic packages where sample edges scatter acoustic energy leading to dark annular regions around the solder bump. This is clearly seen from the ultrasonic C-scan images shown in Fig. 1. The ultrasonic C-scan images in Fig. 1 were produced from the detection of two flip-chip packages soldered on a PCB board [3] using a 230 MHz focusing transducer and gating at the silicon die–solder bump interface. The images labelled as A_0 and B_0 were obtained before thermal cycling while A_{40} and B_{40} were obtained after thermal cycling for 40 thermal cycles. The flip-chip packages contained 109 solder joints. From Fig. 1, it can be seen that the area and intensity of the bright spot at a solder bump inner region increases after thermal cycling. This is due to that thermal cycling causes crack initiation and propagation at the silicon die–solder bump interface. With a larger acoustic impedance mismatch caused by cracks, most of the incident signals are reflected back to the transducer and consequently produce higher intensities. However, how to non-destructively evaluate the crack size

* Corresponding author.
E-mail addresses: cheanshenlee@gmail.com (C.S. Lee), G.Zhang@ljmu.ac.uk (G.-M. Zhang), D.M.Marvey@ljmu.ac.uk (D.M. Harvey), Qiailing1@126.com (A. Qi).

http://dx.doi.org/10.1016/j.ndteint.2015.11.007
0963-8695/

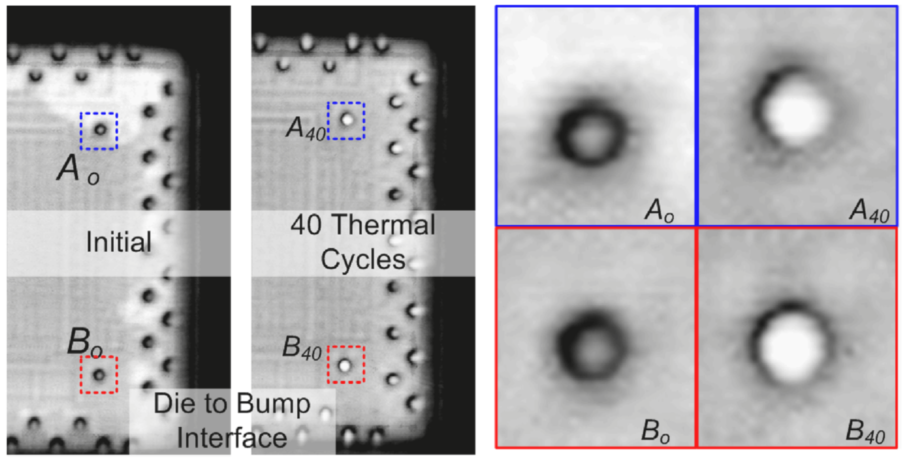

Fig. 1. Edge effect in ultrasonic C-scan images of the silicon die–solder bump interface produced from the detection of two flip-chip packages soldered on a PCB board using a 230 MHz focusing transducer. A_0 and B_0: before thermal cycling; A_{40} and B_{40}: after thermal cycling for 40 thermal cycles.

is a big challenge due to the limited resolution of acoustic imaging and the existing of edge effect. In this paper, a crack propagation characterization method is proposed, which is achieved through exploiting the relationship of the edge effect and the crack size.

2. Finite element modelling for acoustic microimaging of microelectronic packages

Finite element modelling for acoustic microimaging of microelectronic packages was carried out in our previous research to investigate the acoustic wave propagation inside a package and the generation mechanism of edge effect [8,9]. The numerical model was built on the basis of acoustic microimaging of the physical Flip Chip test sample used in our practical experiments. Two dimensional modelling was carried out using ANSYS APDL. The model schematic is shown in Fig. 2. The numerical model consists of three parts: 1) the flip-chip modelled by a solder bump connecting to the silicon die through the Under Bump Metallization (UBM) structure. The composition of the UBM structure is based on [10]. 2) The water medium. The model is submerged in the water medium for simulation of immersion ultrasonic imaging. 3) A Virtual Transducer (VT) attached to the top of the model. The VT is modelled based on the 230 MHz focused transducer used in our experiments. The displacement loads on the VT curve are vectored to mimic a travelling pulse ultrasonic waves very close to the sample. The same VT curve is used as a receiver to collect the reflected ultrasonic waves. In water, the VT produced a spot size of 16 μm and a focal depth of 186 μm which is in close agreement with the physical transducer with a spot size of 15 μm and a focal depth of 192 μm. The mechanical scanning in acoustic imaging of the flip chip package is implemented in the simulation by laterally moving the flip-chip at 1 μm increment. Moving the flip-chip package is equivalent to scanning the transducer. At each scanning position, the entire model is solved to obtain an A-scan signal. The resultant A-scans at different scanning positions are assembled to create a B-scan image with a resolution of 1 μm per pixel on the lateral *X*-axis. The B-Scan is a cross-sectional image of the flip chip. The detailed parameters of the FEM modelling undertaken to describe the contrast in the UT-imaging of solder bumps using an SAM can be found in [8].

To simulate crack propagation, a crack is modelled by the introduction of an air gap with a thickness of 2 μm inside the solder bump. The crack length propagates at an increment of

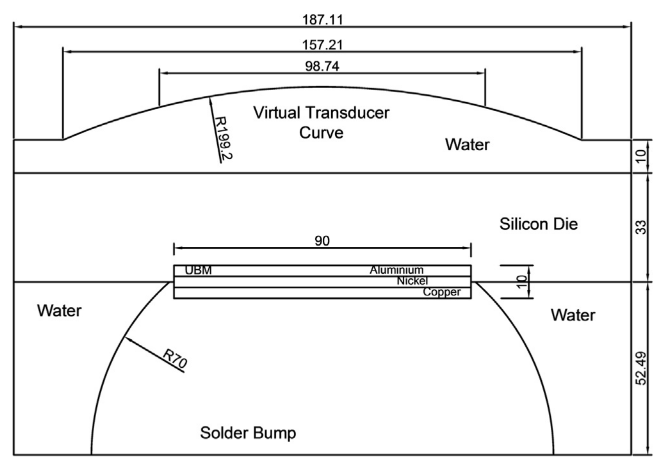

Fig. 2. Numerical model schematic for acoustic imaging of a flip-chip package. Unit: μm.

2.5 μm. The initial and end positions of the crack propagation are illustrated in Fig. 3.

3. Characterization of crack propagation through analysis of edge effect

Fig. 4(a) shows a simulated B-scan image. Since the solder bump structure is symmetrical, only half of the flip-chip show in Fig. 2 is scanned and shown in Fig. 4(a). The position of 0 μm on the lateral *X*-axis in Fig. 4(a) represents that the transducer located on the centre axis of the solder bump. Similar to the C-scan imaging, a C-Line plot can be obtained from the B-scan image by gating the B-scan image at a desired interface. At each transducer position, the biggest amplitude in the gated A-scan signal is taken as the amplitude in that transducer position of the C-line plot. Fig. 4(b) shows the C-line plot obtained from the B-scan shown in Fig. 4(a) by gating interface between 40 ns and 60 ns.

Using the finite elemental modelling described above, a number of simulations were carried out to monitor the crack propagation by the resultant B-scan images. C-Line plots were then obtained from these simulated B-scan images for the silicon die–solder bump interface. Fig. 5 shows the C-Line plots for different size of cracks. The initial crack is set as 25 μm as shown in Fig. 3(a).