Engineering Applications of Artificial Intelligence 26 (2013) 1479–1486

Contents lists available at SciVerse ScienceDirect

Engineering Applications of Artificial Intelligence

journal homepage: www.elsevier.com/locate/engappai

Brief paper

An intelligent system for wafer bin map defect diagnosis: An empirical study for semiconductor manufacturing

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ARTICLE INFO

Article history:
Received 2 August 2012
Received in revised form
21 November 2012
Accepted 25 November 2012
Available online 23 December 2012

Keywords:
Wafer bin map (WBM)
Semiconductor manufacturing
Yield enhancement
Spatial statistics test
Cellular neural network (CNN)
ART 1 neural network

ABSTRACT

Wafer bin maps (WBMs) that show specific spatial patterns can provide clue to identify process failures in the semiconductor manufacturing. In practice, most companies rely on experienced engineers to visually find the specific WBM patterns. However, as wafer size is enlarged and integrated circuit (IC) feature size is continuously shrinking, WBM patterns become complicated due to the differences of die size, wafer rotation, the density of failed dies and thus human judgments become inconsistent and unreliable. To fill the gaps, this study aims to develop a knowledge-based intelligent system for WBMs defect diagnosis for yield enhancement in wafer fabrication. The proposed system consisted of three parts: graphical user interface, the WBM clustering solution, and the knowledge database. In particular, the developed WBM clustering approach integrates spatial statistics test, cellular neural network (CNN), adaptive resonance theory (ART) neural network, and moment invariant (MI) to cluster different patterns effectively. In addition, an interactive converse interface is developed to present the possible root causes in the order of similarity matching and record the diagnosis know-how from the domain experts into the knowledge database. To validate the proposed WBM clustering solution, twelve different WBM patterns collected in real settings are used to demonstrate the performance of the proposed method in terms of purity, diversity, specificity, and efficiency. The results have shown the validity and practical viability of the proposed system. Indeed, the developed solution has been implemented in a leading semiconductor manufacturing company in Taiwan. The proposed WBM intelligent system can recognize specific failure patterns efficiently and also record the assignable root causes verified by the domain experts to enhance troubleshooting effectively.

1. Introduction

Semiconductor manufacturing process is lengthy and technology intensive that contains several hundred process steps with advanced tools to fabricate integrated circuits (IC) on a silicon wafer in the wafer fabrication facility (fab). Semiconductor manufacturing is very capital intensive, in which building a modern 12 in. wafer fab with 40 nm process technologies requires more than 4 Billion USD. Therefore, fast ramp up for new process technology and quick response to yield excursion for strict quality control is crucial to maintain competitive advantages.

For each fabricated wafer, circuit probe (CP) test is performed on each of the gross dies on the wafer and thus can detect the specific failures with the corresponding bin values. The CP yield is one critical yield measure in semiconductor manufacturing (Cunningham et al., 1995), since only the known good dies of the CP test can be packaged into chips for further usage. WBMs are spatial results of CP test presenting specific patterns that experienced engineers can recognize them to track the corresponding process failures in semiconductor manufacturing. Hence, the troubleshooting of low CP yield depends on two steps: recognizing the WBM patterns and identifying the assignable root causes.

In practice, most companies rely on experienced engineers to analyze WBM, while it is time consuming and unreliable for an engineer to cluster the patterns with their eye-ball analysis. Furthermore, the identification of the possible root causes from the specific WBM failure patterns is affected by the domain knowledge and the experience for trouble shooting of the engineers.

A number of studies have applied data mining techniques for trouble shooting and yield enhancement for semiconductor manufacturing (Ooi et al., 2012; Chien et al., 2010, 2007; Wang, 2008; Chien and Chen, 2007; Wang et al., 2006; Palma et al., 2005; Chen et al., 2000). To enhance CP yield, Wu and Zhang (2010) proposed a novel fuzzy neural networks with considering the number of defects per wafer, mean number of defects per chip, mean number of defects per unit area, clustering parameter, chip size

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0952-1976/$ - see front matter © 2013 Published by Elsevier Ltd.
http://dx.doi.org/10.1016/j.engappai.2012.11.009

and five critical electrical test parameters as the input variables. In addition, Self-Organization Map (SOM) clustering has been applied to cluster *E*-test, CP fail bins and metrology data to detect the failure patterns (Chien et al., 2003). Langford et al. (2001) presented a robust windowing method for the Poisson yield model to extract the systematic and random components of yield from wafer probe bin map data. For WBM clustering problems, Friedman et al. (1997) defined four defect clustering patterns including random, edge, top and bull's eye pattern, but give no information about pattern types. For example, mask misalignment in the lithographic process generates a checkerboard pattern; the abnormal temperature control in the rapid thermal annealing process (RTP) can generate a ring of failing chips around the edge of the wafer; the zone pattern often arises from the thin film deposition (Chien et al., 2002). Hsu and Chien (2007) proposed a hybrid data mining approach that integrates spatial statistics and ART neural networks to extract patterns from WBM and associate with manufacturing defects. Wang (2009) proposed an approach that combined spatial statistics, kernel based eigen-decomposition and support vector clustering to estimate the number of defect clusters, and separate the convex and non-convex defect cluster on WBMs.

However, as wafer size is enlarged and IC feature size is continuously shrinking, WBM patterns become complicated due to the different die sizes, wafer rotation, the variant density of failed dies. Motivated by the needs in real setting and improved via empirical studies, this research developed a WBMs clustering solution that integrates the spatial statistics test, cellular neural network (CNN), ART1 neural network, and moment invariant (MI) for the clustering of WBM failure patterns automatically and efficiently. Furthermore, we also constructed an intelligent system for WBM defect diagnosis system equipped with user-friendly graphical interface to help the engineers detect the root cause and the knowledge database to record the know-how and domain knowledge. In particular, a number of WBMs of the twelve patterns defined by domain engineers were used for validation, in which four performance indexes were employed to compare the proposed approach with the other clustering methods. The results have shown that the clustering performance of the proposed approach is superior to other methods. Indeed, the developed solution has been implemented in a leading semiconductor manufacturing company in Taiwan.

The rest of this study is organized as follows: Section 2 introduces the CP yield and the WBMs. Section 3 outlines the proposed system. Section 4 describes an experiment for the proposed pattern clustering system. Section 5 concludes this study with discussions of the results and future research directions.

2. CP yield and wafer bin maps

Yield is a widely used performance measure in semiconductor manufacturing. Sampling test is the way to monitor the production quality during wafer fabrication. In the circuit probe (CP) testing that involves testing of individual die for functionality using different electrical probes and provides key information about the performance of the wafer fabrication process (Chien et al., 2011). Then, the wafers are died up, and the good dies are package into chips and shipped to the customer (Kumar et al., 2006; Hsu and Chien, 2007).

There are three kinds of yields in a semiconductor manufacturing: line yield, CP yield, and final test yield (Cunningham et al., 1995). Among them, CP yield is the critical factor of the manufacturing yield and divided into two major categories. One is base line yield improvement; the other is low yield trouble shooting. Wafer bin maps (WBM) are the result of CP inspection of dies on the wafer at the end of fabrication. They are multi-dimensional and have complex structures, can provide essential information for engineers to identify problems in the manufacturing process. WBM patterns can provide information to monitor the process and product. Fig. 1 shows a typical WBM where the different symbols denote chips failing in different functional tests.

The failure patterns of WBM can be classified into three major categories (Stapper, 2000; Taam and Hamada, 1993):

(1) Random defect: No spatial clustering or pattern exists, and the defective chips are randomly distributed in the two-dimensional map. Random defects are usually caused by the manufacturing environmental factors. Even in a in a near-sterile environment, particles cannot be removed completely. However, reducing the level of random defects can improve the overall productivity of wafer fabrication.
(2) Systematic defect: The positions of defective chips in the wafer show the spatial correlation, for example, ring, edge-fail, checkerboard. Fig. 2 shows ten systematic patterns that are frequently seen in fab, as defined by domain experts.
(3) Mixed defect, consisting of a random defect and a systematic defect in one map. Most wafer maps are of this type, as shown in Fig. 3. Engineer needs to separate random and systematic defects in the WBM, since the systematic defect's signature can reveal the process problem (Friedman et al., 1997).

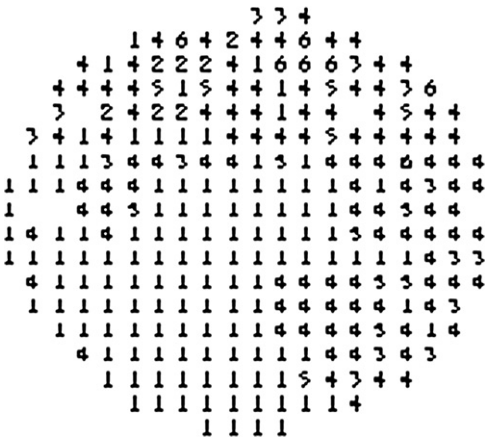

Fig. 1. Defect map and bin map.

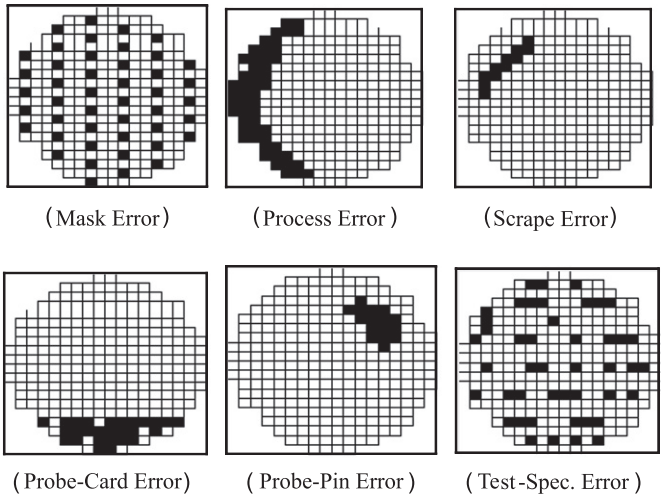

Fig. 2. Six different root cause of wafer map pattern.