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A design process of switched Ethernet architectures according to real-time application constraints ☆

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Abstract

Ethernet networks are based on a medium access method which is not deterministic. The use of such networks in factory environments (which are strongly time constraints) can absolutely not guarantee that the applications requirements will be respected. This paper presents a method based on genetic algorithms to minimize end-to-end delays by providing a good distribution of the devices on the network switches. The objective function is defined by using the network calculus which is a deterministic theory and enables to determine bounded delays. In this paper, a case study is described: theoretical results are verified by a real experimentation and compared with results obtained with a network simulator.

Keywords: Real-time communications; Ethernet; Genetic algorithms

1. Introduction

The industrial communications are currently based on specific networks called fieldbuses such as FIP, Profibus (CENELEC, 1996), CAN. They interconnect Programmable Logical Controllers (PLC), CNC, robots, etc., to exchange technical data for monitoring, controlling, and synchronizing industrial processes. Their main characteristic is to ensure that the end-to-end delays of messages remain limited, compared with the time-cycle of the applications. Thus, these networks are deterministic and some protocols satisfy the integrity constraints of the information. In opposition, the Ethernet networks based on the CSMA/CD protocol are more and more used to interconnect industrial devices. Some applications confirm this evolution in different industrial areas: cars (Jaguar), pharmaceutics (Boehringer Ingelheim), avionics (Grieu et al., 2003), etc. Moreover, different organizations such as the Industrial Automation Networking Alliance (IAONA), the Industrial Ethernet Association (IEA) promote Ethernet as "the standard in the industrial environment". Finally research projects such as CIDER (Alves et al., 2000) study the use of Ethernet as an enabling technology for future dependable real-time systems.

To interconnect Ethernet switches, different topologies can be used. Rüping et al. (1999) shows that the hierarchical topology (Fig. 1) is the most efficient and therefore mainly used in factory networks. Industrial devices are distributed on second level switches which are directly connected to a federative switch. Moreover, this topology will support two supplementary mechanisms: full-duplex communications and micro-segmentation. The reason is that on shared Ethernet networks, collisions could occur, which is a non-deterministic issue. Now with micro-segmentation, each device is isolated in its own segment, so that with full-duplex, collisions are eliminated. In these conditions, the collision problem is shifted to congestion in switches. Thus the objective will be to control and to evaluate the switches congestion.

We propose to design a switched Ethernet architecture which satisfies the time requirements. Our objective is to optimize the network organization at the physical layer

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level. Switched networks design consists in distributing industrial devices on the different Ethernet switches in order to reduce the load of the backbone and of the switches. Fig. 2 shows well that the distribution of the devices on the second level switches mathematically corresponds to the partitioning of the communication graph of these devices as described in Section 2. As the graph partitioning is an NP-complete problem the Genetic Algorithms are suitable to solve this network segmentation problem. The Genetic Algorithms have already been used for networks performance optimisation (Krommenacker et al., 2002, 2001).

The objective is to collect on the same switches the devices which exchange information. Thus, the criterion to minimize is the number of the graph edges cut by the partition. Indeed the end-to-end delay of a message exchanged between two actors belonging to the same partition will be reduced, because the number of crossed switches is minimized. Nevertheless, even if this delay is optimized, it is not guaranteed that it is lower than the application time constraints. That is why the optimization criterion has to explicitly take into account this delay, and more particularly in the worst case. The Network Calculus theory introduced by R. Cruz (see Cruz, 1991a,b) enables to compute an upper-bound of the delay. It is presented in Section 4 and validated with a real experimentation.

Finally, the network design approach described in this paper is illustrated on a factory communication scenario. The obtained solution is evaluated on a real experimentation and with a network simulator. The results show the segmentation impacts on the temporal performances. Therefore, it is important to have a method to design a switched Ethernet industrial network in order to make it deterministic under some specific hypothesis.

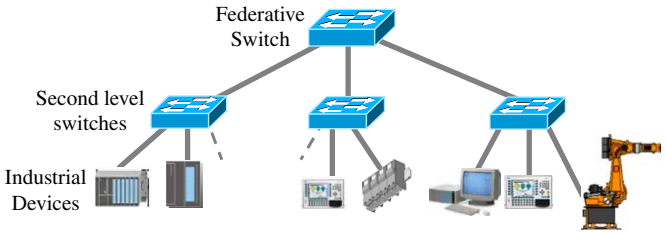

Fig. 1. Hierarchical topology for switched Ethernet networks.

2. Partitioning problem

2.1. Problem

The graph theory is often used to study networks topology. It is obviously true for switched Ethernet networks as shown by Fig. 3 where the dot line represents the distribution of the devices on the two second level switches. In the graph, each industrial device is represented by a vertex and the network communication by an edge between two vertices, i.e. two devices. A partition of this graph will correspond to the mapping of the industrial devices on the different switches.

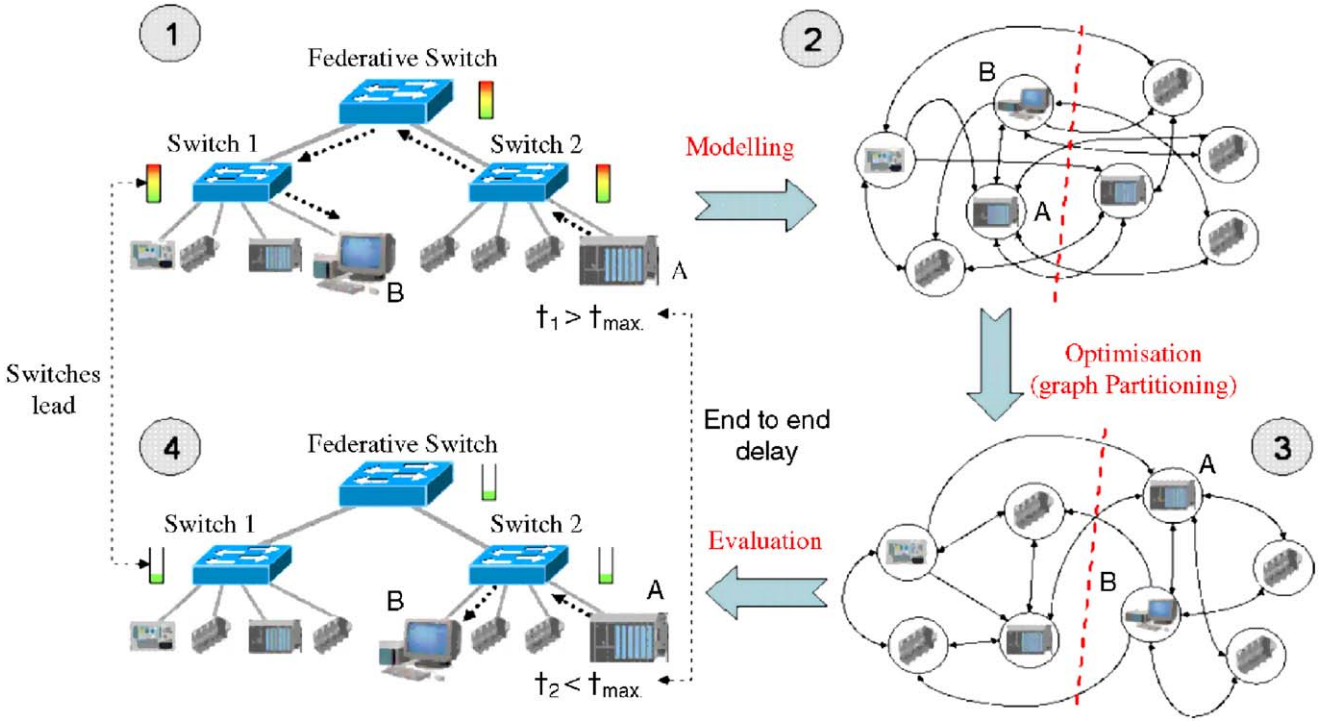

Fig. 2. The segmentation problem is a graph partitioning one.