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# Bacterial foraging driven exploration of multi cycle fault tolerant datapath based on power-performance tradeoff in high level synthesis

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ABSTRACT

Technology evolution and energy of particle impact both plays a major role in inducing multi-cycle transient fault (longer duration transient) in a device. However, designing an optimized multi-cycle fault tolerant system is non-trivial. This paper presents a novel design space exploration (DSE) approach for multi-cycle transient fault tolerant datapath based on user power-delay constraints during high level synthesis (HLS). To the best of the authors' belief, this is the first work to solve this problem in the literature so far. More specifically, the current work in the literature so far utilizes 'triple modular redundancy (TMR)' to design a fault tolerant datapath, however, this paper proposes a 'dual modular redundancy (DMR) design with equivalent circuit' scheme to achieve the same. The novel equivalent circuit that works with DMR systems performs the function of extracting the correct output from the DMR design. Further, the proposed work is the first work in the literature that handles multi-cycle transient faults during design space exploration of fault tolerant datapath. Therefore, key contributions of this paper are as follows: (a) novel multi-cycle transient fault tolerant algorithm that has capability to isolate original and duplicate units in a DMR with respect to the transient fault; (b) novel DSE approach that combines our fault tolerant algorithm along with user specified conflicting power-performance constraint that guides this intractable search problem to reach an high quality fault tolerant solution without violating the power budget and delay requirement; (c) integrates a heuristic based on bacterial foraging optimization algorithm (BFOA) that performs adaptive searching. Finally, results indicated an average improvement in Quality of Results (QoR) of >24% and reduction in hardware usage of >57% of the final solution compared to similar approach.



## 1. Introduction

With the ever changing trends in technology and competition faced in the emerging market, designers are focusing at optimizing Very Large Scale Integration (VLSI) designs by performing exploration during HLS. HLS involves transition of a behavioral description of an application into its register transfer level (RTL). This includes an automated process called 'DSE' to explore the best possible design from a set of assorted design alternatives of equivalent functionality. The exploration process is a multi-objective optimization problem which requires a tradeoff between multiple conflicting parameters as well as orthogonal conditions. The traditional focus during this DSE has mainly been on optimizing designs based on delay and power constraint. However, optimizing designs with the above mentioned objectives is no longer sufficient now due to advent of faster devices in current/future technologies. This is because these faster devices of current/future technologies are prone to multi-cycle transient faults due to the idea of packing millions of transistors on a single chip. This increase in density per unit area is negatively impacting the device and overall systems reliability by making it susceptible to transient faults or the single event upsets (SEU) (Normand, 1996) especially in space applications. Transient faults are radiation induced faults which are non-permanent in nature. These nonrecurring faults can be caused by energized particles, environmental noise or electromagnetic interference (Dhodhi, Hielscher, Storer, & Bhasker, 1995; Ferrandi, Lanzi, Loiacono, Pilato, & Sciuto, 2008; Gajski, Dutt, Wu, & Lin, 1992; Haubelt, Schlichter, Keinert, & Mike, 2008; Krishnan & Katkoori, 2006; Micalewicz, 1996; Michel, 1994; Patel, Pradhan, & Koren, 1991; Sengupta & Sedaghat, 2011; Torbe & Knight, 1998; Zeng, Sedaghat, & Sengupta, 2010). The duration of such faults is in order of a few picoseconds (Adler & Templeton, 1967; Doyle & Shoeni, 1984; Karri & Orailoglu, 1996; Lakshminarayana, Raghunathan, & Jha, 2000; Maeda, Imae, Shioi, & Oosawa, 1976; Pierucci, 1972; Williams, Brown, & Zwolinski,

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2008; Wu & Karri, 2004). Therefore, the DSE process in HLS of the future technologies should aim at optimizing reliability besides power and delay. In other words, to achieve high reliability of the designed systems, multi-cycle transient fault tolerance (Choi & Malek, 1988; Geist & Trivedi, 1990; Jou & Abraham, 1988; Lala, 1985; Normand, 1996) should be considered as design metric (or constraint) during multi-objective DSE in HLS (Choi & Malek, 1988; Gajski et al., 1992; Johnson, 1989; Jou & Abraham, 1988; Krishnan & Katkoori, 2006; Lala, 1985; Normand, 1996; Passino, 2002; Wu & Karri, 2001; Zeng et al., 2010). However, there exist no work yet which proposes an adaptive and intelligence DSE system using BFOA for multi-cycle transient fault tolerant datapath (more specifically with an integrated dual modular redundancy design and equivalent circuit scheme) based on power-performance tradeoff.

In this paper, the first multi-objective design space exploration approach is introduced to explore an optimal multi-cycle fault tolerant datapath based on conflicting user constraints. For such a multi-dimensional intractable problem as mentioned above, the search algorithm mapped to solve this problem is BFOA because other evolutionary algorithms such as GA, hybrid GA and particle swarm optimization (PSO) do not provide enough options to incorporate guided/adaptive searching such as change in directions when a certain search path is found unproductive. Further, due to multiple loops involved in BFOA such as chemotaxis and replication as well as options of tumble/swim (helping to change directions when required), the framework of this algorithm provides the flexibility to be configured in an proficient way for eliciting efficient search behavior during multi-dimensional DSE

## 2. Related work

The approaches developed so far are aimed at exploring the design space along with balancing some multi-conflicting issues during generation of the best possible solution (or Pareto front). Over the years the DSE process has evolved where the requirements specified by the user have also convoluted, ranging from simple area-delay tradeoff in initial years to complex power-delay tradeoff in recent years. Further, some HLS approaches just included the consideration of fault security aspect while designing, but without focusing on DSE of fault tolerant designs based on power-performance tradeoff. Nevertheless some recent approaches Haubelt et al. (2008), Lebreton, Coussy, and Martin (2010), Liu and Carloni (2013), Mandal, Chakrabarti, and Ghose (2000), Nestor and Krishnamoorthy (1993), Zhang et al. (2008) are worth mentioning which are efficient DSE approaches/tools however without any consideration on fault aspect during HLS:

For example, authors in Mandal et al. (2000) have applied GA to the binding and allocation phase. A specific crossover technique has been introduced which is based on force directed algorithm. The other limitations of the presented approach besides being unable to handle transient fault, tries to minimize the resource/hardware without considering the power as design objective. Authors in Nestor and Krishnamoorthy (1993) have proposed simulated annealing DSE method called 'SALSA' for optimizing delay which uses many probabilistic search operators to enhance the performance of SA-based technique. However, the other limitations with approaches Mandal et al. (2000), Nestor and Krishnamoorthy (1993) besides being unable to handle transient fault is that it does not consider power during design trade-off. Authors in Lebreton et al. (2010) proposed an approach based on hierarchical and multiple clock domain HLS to target low power design on FPGA. The authors targeted FPGA unlike the proposed approach. Further, this work besides being unable to handle transient fault also does not consider power constraint as it only considers throughput constraint. In addition, Authors in Zhang et al. (2008) introduced a tool called AutoPilot for HLS. It performs C/C++/systemC-to-RTL synthesis. Although this tool performs area-performance-power tradeoff during DSE, however, the tool does not have ability to mask transient fault as well as only targets FPGA's. However, the proposed approach in this paper is fault tolerant as well as it handles power-performance constraints using novel adaptive bacterial foraging driven exploration approach. Furthermore, authors in Haubelt et al. (2008) introduced a tool called SystemCoDesigner that offers rapid design space exploration with rapid prototyping of behavioral systemC models. An automated integrating approach is developed by integrating behavioral synthesis into their design flow. However, the approach besides being unable to handle transient fault, is also limited to area-delay tradeoff. In addition, authors in Liu and Carloni (2013) propose a machine learning method for DSE which introduce a transductive experimental design that can wisely sample micro-architecture choices and use them for training in the learning model. However, besides being unable to overcome faults it does not consider power during exploration. Additionally, authors, in approach Williams et al. (2008) also used simulated annealing to generate optimum results; however, the work did not consider transient fault detection and correction during exploration. But the proposed approach presented in this paper besides considering power and execution time (or delay) as design objective during exploration, also considers multi cycle transient faults during optimal datapath generation. Therefore, it ensures an optimal fault tolerant datapath generation after exploration based on conflicting user constraints. Further, the proposed framework is also driven by an intelligent searching called bacterial foraging optimization algorithm which incorporates multiple loops such as chemotaxis tumble/swim to handle efficient guided searching during exploration.

Additionally, by far there have been no approaches developed which concurrently propose a multi-objective design space exploration process of a multi-cycle (or single cycle) fault tolerant design during HLS. A complete fault tolerant system should possess different capabilities. Depending upon the fault tolerance level required it should be capable of identifying the fault, detecting it, followed by its isolation, masking and then recovering from it. The fault detection technique involves the redundancy factor to identify the faults prevailing in the system. It either uses the hardware redundancy or the time redundancy (Choi & Malek, 1988; Karri & Orailoglu, 1996; Normand, 1996) or a combination of both to determine the presence of fault within a system. Therefore, exploration of a multi-cycle fault tolerant datapath for conflicting user constraints becomes non-trivial.

In the literature so far, only one approach has been proposed by authors in Inoue, Henmi, Yoshikawa, and Ichihara (2011) who discussed a HLS approach for multi-cycle transient fault tolerant datapath. However, there was no algorithm for exploration of an optimal fault tolerant datapath based on power-performance constraint as presented in the paper. Further, the authors did not provide any concept of multi-cycle transient fault during DSE. Moreover, the approach presented a TMR (triple modular redundant) system for $k$-cycle fault tolerance for single event transient (SET). The outputs of the units were voted upon by the help of voter, to mask the errors. Additionally, comparators were used to detect the difference in the outputs of the units. However, the proposed approach uses Double Modular Redundancy (DMR) scheme to explore a fault tolerant design without using voters to extract the correct output. Therefore, Inoue et al. (2011), involved higher redundancy which sometimes involved TMR system with tripled resource usage.

Besides above, only efforts have been made as underlined below which solely deal with the error detection issue of the designs without ability to isolate the fault as well as explore optimized