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CMOS fuzzy logic controller supporting fractional polynomial membership functions

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Abstract

This paper presents a new Fuzzy Logic Controller (FLC) having the ability to support fractional polynomial membership functions. These functions are general forms of triangular and trapezoidal membership functions, and also those functions which are used in linguistic hedge FLC (LHFLC). A two-input, single-output Takagi–Sugeno–Kang (TSK) type 0 FLC is designed in 0.35 μm standard CMOS process. Analog realization of the circuit makes the design programmable and extendable, while having high speed and low power consumption. Also all the control signals and input signals are in voltage form and no need for digital programmability. Voltage mode realization of the circuits leads to a simple use of FLC with other circuits which are in voltage mode like sensors. Simulation results of the controller using HSPICE simulator and BSIM3v3 parameters, and comparing them with ideal results obtained from MATLAB software verify the functionality and performance of the design.

Keywords: Fuzzy controller; Fractional polynomial membership function; Takagi–Sugeno–Kang

1. Introduction

In Ref. [1], the fractional polynomial membership functions are introduced and optimized using Extended Kalman Filter (EKF) algorithm. These functions are general forms of triangular and trapezoidal wave forms and also those functions which are applied in LHFLC [2]. Realization of a TSK type FLC is easier and more efficient than the Mamdani type [3]. Hardware requirements of such controllers are lower, as well as computational complexity and power consumption [2]. In this paper, design of a two-input single-output sixteen-rule TSK type FLC is described. It is realized in voltage-input current-output type zero. This controller can support fractional polynomial membership functions and generate powers of 0 up to 4 with continuing resolution and it can be also used as an LHFLC. The block diagram of the controller is described in Section 2, followed by the transistor level design of its several blocks in Section 3. In Section 4 the layout of the controller is shown. In Section 5, simulation results for each block and

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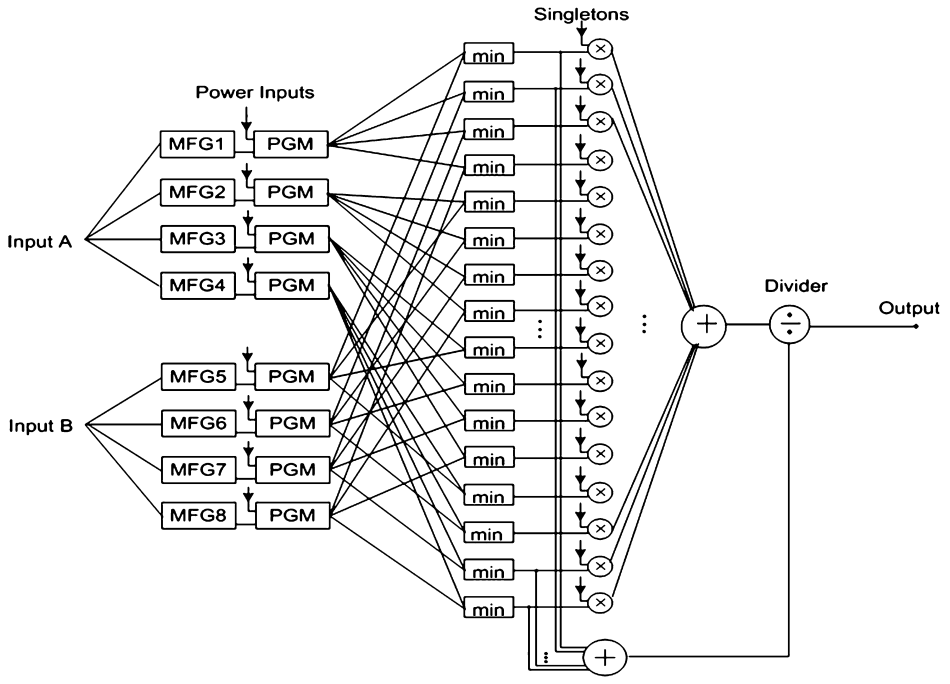

Fig. 1. Complete block diagram of proposed FLC.

also the complete controller using HSPICE simulator are presented, and are compared with the results of MATLAB software to show the efficiency of the design. Finally Section 5 concludes the paper.

2. Functional block diagram

The complete block diagram of proposed FLC is shown in Fig. 1. Each fuzzifier consists of a tunable Membership Function Generator (MFG), followed by another block named Power Generator Module (PGM). The universe of discourse of inputs is partitioned into 4 regions (fuzzy sets) as shown in Fig. 1. After generating a conventional membership function by the first block, the PGM generates a user tuned power of it.

In hardware realization of a controller, the rule-base is usually a set of IF-THEN rules which are determined by the user, and the controller must provide capability of programming this block. Because the controller has two inputs and four fuzzy sets for each block, total number of rules is considered to be 4×4 rules.

Note that because of current-mode output, the summation of signals is done by a simple wiring to a low impedance node and is not discussed in hardware implementation. Finally, the defuzzification is simply a division operation, which performs center of sums method (similar to center of gravity for Mamdani type FLC [2]), that is, dividing the sum of implied singletons over the sum of firing values:

$$y = \frac{\sum_{i=1}^{M} w_i X_i}{\sum_{i=1}^{M} w_i} \tag{1}$$

where y is the defuzzified (crisp) output, M is the number of rules, w_i is the singleton of ith rule, and finally X is a function of inputs $X = f_j$ (*inputs*).

In the next section, a detailed discussion of the blocks and their circuits is presented.

3. Circuit design of proposed FLC

To produce proposed FLC we need a tunable fuzzifier (MFG), a power generation module (PGM) and minimum current selector, multiplier and divider circuits.