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An improved Dynamic Voltage Restorer for power quality improvement

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A R T I C L E I N F O

ABSTRACT

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Keywords: Voltage harmonics RLC filter Voltage sag Cascaded H-Bridge inverter The capacity of the voltage source inverter (VSI) and the values for the link filter connected between the injection transformer and the inverter play a crucial in the design of the DVR. In this research paper, new Dynamic Voltage Restorer (DVR) topology has been proposed. The capacity of the voltage source inverter (VSI) and values of the link filter is small that will improve the compensation capabilities for voltage harmonic, swell and voltage sag mitigation under various fault conditions. The new RLC filter is able to eliminate the switching harmonics. The capacity of the dc supply voltage is reduced when the value of inductance is small. The new DVR topology has high efficiency and the ability to improve the quality of voltage. An outline architecture of the RLC filter parameters for the specific model has been presented. The new DVR topology is modeled and simulated using the PSCAD/EMTDC. The control scheme has good control dynamics with minimum transient current overshoot. The simulation results under transient performance are good.

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Introduction

The typical loads used in most of the industrial and commercial applications are power electronic based. The usage of these devices is due to the improvements in semiconductor devices, the controllers and methods to control the power usage. The problems associated with these devices are: poor power factor, voltage harmonics and large neutral current due to third harmonic [1]. Some of the power electronic devices are very sensitive to voltage sag and swell. Voltage imperfections will cause disruptive equipment operation. The shunt passive filters are commonly connected at the load end to block harmonics. These passive filters are able to suppress the 5th and 7th harmonics but are bulky dimensions and will cause resonance problems [1,2]. To mitigate current harmonics, the shunt active power filters (SAPF) are proposed [3,4].

The series connected DVR is effective to restore the quality of voltage at the sensitive load end [5]. The DVR consists of VSI, dc supply, series injection transformer and smoothing filter [6,7]. The DVR power is related to the supply voltage and the real power supply available. For improved performance, the capacity of the real power is equal to or higher than the system phase voltage for traditional topology. However, this has an impact on the voltage and current level of the VSI. This also affects the sizing of the

RLC values. The price, dimension, weightiness, and capacity of VSI are increased. The nature of the injected current of the VSI depends on the inductor L. Small value for inductor L indicates reduce voltage drop through it. Also, the low value of the dc power supply is required for proper compensation. The slew rate of the current through the inductor is limited by the inductance. Small value of inductor L helps in improving the system response to the load transient.

The series connected DVR will inject three-phase compensating voltages through the three-phase injection transformer or three single-phase injection transformers with the main supply. The filtered VSI output voltage is boosted to the desired level with the injection transformer. The transformer also isolates the DVR circuit from the distribution system.

The real power energy required for the compensation is taken from the dc power supply [8,9]. In [10,11] researchers have used a hybrid filter model with shunt passive filters tuned at seventh harmonics. In [12] a series inductor L is connected to reduce the dc supply bus voltage. However, increase voltage drop in L will affect the dc supply bus voltage. This is not an economical and cost effective solution.

A new DVR is proposed combining the advantages of the RLC filter with 3 single-pole 7-level H-bridge VSI for improved performance. The improved control scheme uses synchronous reference frame controller algorithm with zero-sequence connection for unbalanced fault. The Phase Shifted Pulse Width Modulation signals control the gating signals for the 7-level H-Bridge VSI. The







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RLC dimensions are much smaller in the new topology. The capacity of the VSI provides an excellent performance, simultaneously.

An improved DVR topology

The traditional DVR topology is shown in Fig. 1. Three independent single-phase three level mid-point clamped voltage source inverter is used. The size of the dc power supply is large and affects the value of the LC interface filter connected between VSI and the injection transformer. The source voltage and source currents are Vsabc and Isabc for the phases a, b, and c respectively. The voltages and currents at the load end are denoted as VLabc and ILabc. The sensitive loads at the consumer end are nonlinear elements. The proposed DVR topology is shown in Fig. 2.

The RLC filter with reduced dimension enhances the reference tracking functioning.

The resistance R is connected in series with L and in parallel with capacitor C. This will stifle out resonance amplitude to the entire system. A 7-level H-bridge connected inverter is used to improve the performance of the DVR. Unlike the flying or clamping diode types, for the cascaded H-Bridge (CHB) configuration the total input power is distributed equally among the cells of different input sources.

Another specialty of the CHB inverter is that the inverter can still be operated at reduced power level even with one cell is operative [13].

Distribution system with proposed DVR

The DVR is series connected with the power supply and the protected sensitive load is shown in Fig. 3.

The DVR controls the quality of voltage at the sensitive load against voltage deformities. The voltages Vs, PCC, VLoad, Vinj and Pinj denotes the grid, point of common coupling, load voltage, injected voltage and the power injected respectively, and Is is the grid or the supply current as shown in Fig. 3. The proposed DVR has the following advantages:

Each phase is independently controlled. Each block of H-bridge has its own dc source. Improved and accurate compensation capability of DVR.

In this research project, the seven-level cascade multilevel inverter topology with the multicarrier based Phase Shift Pulse Width Modulation (PSPWM) controller strategy are selected for the development and control of the DVR module. The PWM based

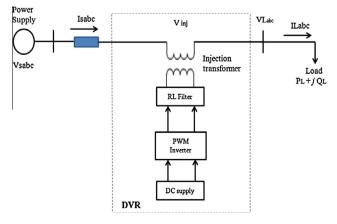


Fig. 1. Traditional DVR topology.

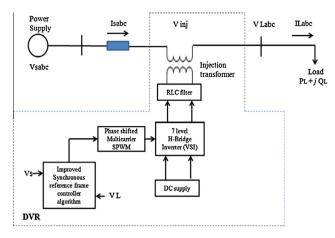


Fig. 2. Proposed DVR topology.

DVR control technique with fast switching speed; the layout is simple with good dynamic response. The efficiency of the converter can be improved with high switching frequency with minimum switching losses [14]. The basic idea of PWM based multicarrier phase shift modulation technique is by varying the ON or OFF switching periods of the IGBTs switches at a constant frequency so that the ON periods are the longest at the peak of the wave. The control of switch duty ratio adjusts the output voltage level.

RLC filter system

The single-phase schematic symbol of an inverter system is shown in Fig. 4. Einv is the VSI output voltage, supply current is ix, current through capacitor is ic, load current is iL and VL is voltage across the load.

Assuming the dc supply voltage Vdc is constant and the gate switch of VSI is ideal. Based on Fig. 4, the output voltage of the VSI is written as;

$$\operatorname{Einv} = \operatorname{VL} + \operatorname{Rix} + \operatorname{L} \frac{d\mathrm{ix}}{dt} \tag{1}$$

The voltage within the capacitor VL and current inside the inductor ix can be separated into the average over a switching cycle and harmonics ripple components, that is,

$$VL = \overline{VL} + \widetilde{VL}$$
(2)

$$ic = \overline{ix} + \widetilde{ix}$$
 (3)

Eqs. (2) and (3) into Eq. (1) gives,

$$\operatorname{Einv} = \overline{\operatorname{VL}} + \widetilde{\operatorname{VL}} + \operatorname{R}(\overline{\operatorname{ix}} + \widetilde{\operatorname{ix}}) + \operatorname{L}\frac{d}{dt}(\overline{\operatorname{ix}} + \widetilde{\operatorname{ix}})$$
(4)

For good filter designed, the values of $\tilde{V}L$ and Rix are small compared to $L_{dt}^{\underline{dix}}$ and therefore, the ripple component of the filter inductor current becomes

$$\widetilde{ix} = \frac{1}{L} \int (\text{Einv} - \overline{\text{Einv}}) dt$$
(5)

and the mean or average value of output voltage is

$$\operatorname{Einv} = \overline{\operatorname{VL}} + \operatorname{Rix} + Ldix/dt \tag{6}$$

With reference to Fig. 4, the voltage harmonic of capacitor; ic = ix - iL (7) Download English Version:

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