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Sub-module component developed in CBuilder for MMC control and protection test in RTDS

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ABSTRACT

Modular multilevel converter (MMC) is one of the most promising direct-current (DC) transmission modules. To establish a flexible sub-module model in RTDS for evaluating the protection and control devices is important and useful for the fast development of MMC-HVDC technology. A component for the sub-module, rtds_SM, is proposed in this paper, which is developed by CBuilder in RTDS to provide a flexible and available model to test the control and protection devices for MMC system. First, the rtds_SM component, considering the bypass switch branch, is established by using CBuilder in RTDS. It has seven inputs and two outputs, which can response to various operation states under various conditions. The information of the capacitor voltage balancing is calculated in the component and output as a variable. Second, the memory usage and the simulation precision of the proposed model are analyzed in detail. It is suitable for the simulation in RTDS if the carrier frequency is smaller than 1.2 kHz. Third, the steady states and transient states are tested for the rtds_SM proposed in this paper. Numerical results show that it meets the requirements for various operating conditions. The proposed component has been successfully used to test the controller and protection devices designed by Xian XD Power Systems Co., Ltd. for a practical MMC system in China.

1. Introduction

With the development of renewable energy, VSC has been developing rapidly for its flexibility and high controllability [1,2]. However, the conventional VSC, which is based on two-level or three-level converter [2], has high switching losses because of the high switching frequency. Moreover, the higher harmonics, the limited voltage level and the difficult voltage balancing between devices [3] are disadvantages of the conventional VSC system.

MMC has drawn much attention in recent years [4–11]. The flexible topology structure of MMC leads a way to solving the problems caused by the conventional VSC [4]. The study on MMC is mainly focused on the mathematical models [5–7], capacitor voltage balancing control [8–11] and modulation strategy [10–15].

An efficient MMC model based on time-varying Norton equivalent circuit [5] is proposed to reduce the number of the nodes for the calculation in simulation. A generalized mathematical model for MMC under balance and unbalance conditions is established by using sequence component method [6]. PD-SPWM strategy [8,9] are proposed to solve the problems of voltage balancing. The capacitor voltage balancing is theoretically analyzed and an additional control is proposed in [10]. MPC is proposed to eliminate the circulating currents [11] by using the redundant switching states. The space vector PWM strategy for MMC [12,13] is widely used for the modulation method of MMC system. The NLC [14] is proposed to reduce the THD.

The topology construction of the three-phase MMC is shown in Fig. 1. It contains 6 bridge arms and each arm consists of many SMs and a reactor, *L*, connected in series [4].

The mainly construction of SM is shown in Fig. 2. $IGBT_1$ and $IGBT_2$ are insulated gate bipolar transistors. D_1 and D_2 are antiparallel-connected diodes. *C* is the capacitance of the capacitor. V_c is the voltage of the capacitor. V_{sm} is the output voltage of the SM.

There are two ways to establish the MMC system in RTDS: (1) Establish the MMC system with the small step components, and (2) Use the given components in RTDS to build MMC system.

For the former way, the network limitation for small-step systems in RTDS is 30 nodes and 36 switch devices [17]. That is, each bridge arm can only have two SM in a small step encapsulation module at most.

For the latter way, there are three given components for MMC in RTDS: rtds_vsc_MMC4, rtds_vsc_CHAINV3 and FPGA based MMC model.

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Nomenclature

HVDC	high voltage direct current	PWM	pulse width modulation
IGBT	insulated gate bipolar transistor	RTDS	real time digital simulator
MMC	modular multilevel converter	SM	sub-module
MPC	model predictive control	SPWM	sinusoidal pulse width modulation
NLC	nearest level control	THD	total harmonic distortion
PD	phase disposition	VSC	voltage source converter

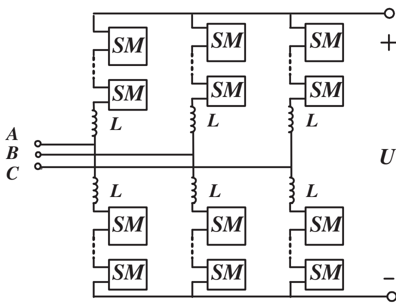

Fig. 1. Three-phase topology of MMC.

The rtds_vsc_MMC4 and rtds_vsc_CHAINV3 components are shown in Fig. 3.

The rtds_vsc_MMC4 and rtds_vsc_CHAINV3 cannot be used to analyze the behavior of the MMC when SMs fault. Furthermore, the rtds_vsc_MMC4 component can only be used in PB5 cards.

The FPGA based MMC model is the latest component for MMC provided by RTDS Technologies Inc. The FPGA based MMC can support up to 512 SMs per arm and can represent some simple faults, such as the value change of the buffer reactor L, the value change of the capacitance of the capacitor and the bypass of the whole arm. However, many kinds of SMs' faults could not been represented by this model, such as: (1) the bypass switch refuses to act, (2) the IGBT could not be fired, and (3) several SMs fail to work and are replaced by the spare SMs, etc.

An rtds_SM component is established in this paper by programming in CBuilder in RTDS. It can be used to test the control and protection devices for MMC-HVDC systems.

The rest of this paper is organized as follows. Section 2 proposes the equivalent circuit of the sub-module of MMC. Section 3 designs the rtds_SM component in detail. Section 4 analyzes the memory usage and the simulation precision of the proposed rtds_SM component. Section 5 shows the simulation results. Section 6 draws the conclusion of this paper.

2. The equivalent circuit of the sub-module

2.1. The SM model with protection circuit

The most important component in MMC is SM. According to the state of $IGBT_1$ and $IGBT_2$, there are three states of SM as shown in Table 1.

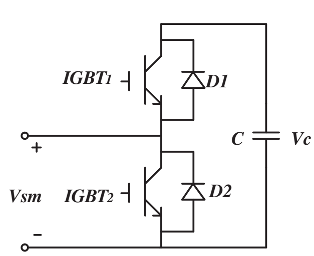

Fig. 2. Structure of SM.

Considering the protection circuit, the SM model consists of 5 elements: bypass switch, thyristor valve, capacitor, IGBT and anti-parallel-connected diode, as shown in Fig. 4.

The bypass switch will be switched on if the corresponding SM faults. The state of the bypass switch is determined by the signal K. The bypass switch is off when $K = 1$ and vice versa. The bypass thyristor valve will be fired by the rising edge of the signal T. There would be several microseconds delay for the action of the bypass thyristor after the rising edge shows up. The protective thyristor switch is fired by the firing pulse T to reduce the current of D_2 if necessary [16].

2.2. The model of capacitor

The relationship between the voltage and the current of the capacitor is,

$$V_c(t) = \frac{1}{C}\int_0^t I_c(t) \tag{1}$$

Linearizing (1) with the trapezoidal integration method [5],

$$V_c(t) = V_c(t-dt) + \frac{dt}{2C}[I_c(t-dt) + I_c(t)] \tag{2}$$

Then,

$$I_c(t) = \frac{2C}{dt}V_c(t) - \frac{2C}{dt}V_c(t-dt) - I_c(t-dt) \tag{3}$$

Therefore,

$$I_c(t) = G_cV_c(t) + I_h(t) \tag{4}$$

where $I_c(t)$ is the capacitor current. $V_c(t)$ is the capacitor voltage. $I_h(t) = -G_cV_c(t-dt) - I_c(t-dt)$ is the equivalent injective current source. $G_c = 2C/dt$ is the equivalent conductance. dt is the simulation time step. Smaller dt leads to higher precision.

2.3. The model of IGBT

Assuming S_1 and S_2 are the switching functions of $IGBT_1$ and $IGBT_2$ respectively, S_1 (S_2) is 1 when $IGBT_1$ ($IGBT_2$) is switched on and S_1 (S_2) is 0 when $IGBT_1$ ($IGBT_2$) is switched off. When the IGBT is switched on, it equals to a small-value resistance R_{on}, such as 10^{-5} Ω. When the IGBT is switched off, it can be considered as a large-value resistance R_{off}, such as 10^5 Ω.

Therefore, the equivalent resistance R_{s1} for the upper switch $IGBT_1$ and the equivalent resistance R_{s2} for the lower switch $IGBT_2$ are,

$$\begin{cases} R_{s1} = S_1 \cdot R_{on} + S_2 \cdot R_{off} \\ R_{s2} = S_1 \cdot R_{off} + S_2 \cdot R_{on} \end{cases} \tag{5}$$

When the SM is inserted, the equivalent resistance of $IGBT_1$ and $IGBT_2$ are R_{on} and R_{off}, respectively,

$$\begin{cases} R_{s1} = R_{on} \\ R_{s2} = R_{off} \end{cases} \tag{6}$$