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Analysis of cascaded multilevel inverters for active harmonic filtering in distribution networks

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ABSTRACT

This paper aims at the investigation of an active power filter (APF) comprised of a transformerless multilevel inverter (MLI) for power conditioning in three-phase three-wire distribution network. The inverter topologies used here are three, five, seven and nine-level. The system configuration mainly involves cascaded MLI structure of APF, generation of compensation filter currents based on instantaneous active and reactive current component (i_d–i_q) method and dc-link voltage regulation using a PI controller. Not many papers focus on the regulation of dc-link capacitor voltage. Here we have proposed the implementation of bacterial foraging optimization (BFO) to extract the gains of PI controller. The proposed work provides improved dc-link voltage regulation, quick prevail over current harmonics and reduction of overall source current THD. Adequate MATLAB/Simulink simulation results are presented for the different cascaded MLIs discussed above. Additionally, the performance has been validated in real-time using Opal-RT Lab simulator considering three different conditions of supply i.e., balanced sinusoidal, balanced non-sinusoidal and unbalanced sinusoidal.

Introduction

A large number of power quality problems associated with current harmonics, are resulted due to the high usage of non-linear loads like power electronic converters, adjustable speed drive systems, fluorescent lights, arc furnaces and many more. APF has gained well recognition as a power conditioning device that consists of semiconductor switching devices. It is designed to filter out all orders of harmonics simultaneously, even when the harmonic content in the current drawn by loads varies randomly. The APFs used in power system are generally comprised of voltage source inverters (VSI) as discussed in [1] and the references there-in.

Literature review and motivation behind the presented work

As the demand for medium and high voltage, high power applications is increasing, the research progress is heading towards multilevel power converters. Nabae et al. first introduced the concept of multilevel converter in the year 1975 [2]. A major disadvantage associated with multilevel converters is requirement of more number of power semiconductor switches, each of which need a related gate drive circuit. This may cause the overall system to be more expensive and complex. Nevertheless, advantages offered by MLIs over conventional two-level VSIs predominantly take over the disadvantages, such as:

(1) Generation of higher voltages with low harmonic content and lower dv/dt distortion, therefore electromagnetic compatibility problems can be reduced.
(2) Two-level inverters have the disadvantages like high-order harmonic noise and additional switching losses due to high-frequency commutation.
(3) Draw input current with very low distortion.
(4) Considerable reduction in size and volume, as no bulky coupling transformers or inductors are required.
(5) Reduce the voltage or current ratings of the semiconductors and the switching frequency requirements, thereby resulting in reduced power loss due to the switching of semiconductor devices.

MLIs when used in APF instead of traditional VSI; can reduce the additional harmonics generated by the APF itself. By increasing the number of levels of MLI, the quality of output voltage waveform can be improved, because the voltage has more number of steps and hence is more close to sinusoidal [3]. MLIs are basically classified into three types depending upon topologies [4], such as:

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(1) *Diode clamped (neutral clamped) inverter:* It is composed of main switching devices operating as switches for PWM and auxiliary diodes to clamp the output terminal potential to the neutral point potential.
(2) *Capacitor clamped (flying capacitor) inverter:* Its structure is similar to diode clamped inverter except the point that, it uses capacitors in place of clamping diodes.
(3) *Cascaded inverter:* Unlike diode clamped and capacitor clamped topologies, the cascaded inverter structure does not require additional clamping diodes or voltage balancing capacitors. A separate dc source is connected to each of the single-phase H-bridges, whose ac terminal voltages are connected in series.

The cascaded MLI was first introduced for motor drive applications [5] and was later used for reactive and harmonic compensation [6]. Further, work has been reported on universal power conditioning of power systems, especially for medium-voltage systems [7,8]. This inverter provides lower costs, higher performance, less electromagnetic interference (EMI), and higher efficiency than the conventional inverter for power line conditioning applications, both series and shunt compensation [9,10]. The cascaded inverter has inherent self-balancing characteristics. However, because of the circuit component losses and limited controller resolution, a slight voltage imbalance can occur.

The most crucial part of designing an APF is the selection of an appropriate control scheme for generation of reference compensation currents. An inexact reference filter current may lead to imprecise harmonic compensation. Out of the numerous control schemes for shunt APFs that exist in literature [11–14], i_d–i_q method is well established as a proficient scheme to mitigate harmonics under all kinds of supply voltages [14,15]. Because, this method utilizes only instantaneous three-phase load currents to generate the reference filter current template, it is independent of the nature of supply voltages.

The dc-link voltage of the inverter must be maintained constant all the time, under any load and supply condition. Despite considerable advance in advanced controllers, the classical PI controller still remains the most preferred controller by the researchers and application engineers [16], owing to its simple structure and robust nature irrespective of the variations in system parameters. However, for efficient performance of APF, the PI controller gains should be properly tuned. In conventional PI tuning methods such as Ziegler–Nichols [17] and Cohen Coon [18], the gains are extracted at a single operating point considering the entire model under study to be a linear one. This indicates that, the same values of PI controller gains will give inadequate results under all other operating points. Various evolutionary computation techniques have been applied in recent times to obtain the optimal PI controller parameters [19–24]. Over certain real-world optimization problems, BFO is believed to outperform other optimization tools such as GA and PSO in terms of speed of convergence and final accuracy [22,23,25,26]. This factor is the motivation behind our presented work that proposes the implementation of BFO technique for the regulation of dc-bus voltage in various cascaded MLIs.

Contribution in the presented work

The objectives of the work presented in this paper may be documented as follows:

(1) To realize the modeling and development of three-phase shunt APFs employing cascaded 3, 5, 7 and 9-level MLIs to showcase the potential advantages of MLI over conventional VSI.
(2) To extract the reference filter currents required to mitigate the current harmonics produced by nonlinear power electronic load using the well established i_d–i_q control scheme.
(3) To regulate dc-link voltage of inverter using a PI controller, the gains of which are optimized using bacterial foraging optimization.
(4) To perform extensive investigations on the proposed implementation of BFO for dc-link voltage regulation of MLI in the shunt APF model in MATLAB/Simulink environment and real-time analysis in Opal-RT Lab; under ideal, distorted and unbalanced supply conditions.
(5) To illustrate the combined advantages of using a MLI topology and BFO-based PI controller in APF application, which results in source currents with well acceptable THDs under both ideal and non-ideal supply conditions, ultimately satisfying the IEEE 519-1992 Standard Recommendations on harmonic limits.

Organization of the paper

The rest of the paper is organized under the following headings. The next section begins with a discussion on shunt APF system configuration with MLI topology, followed by a brief description of i_d–i_q control scheme for generation of required compensation currents. Section 'dc-link voltage regulation' illustrates the regulation of inverter dc-link capacitor voltage, need for optimization and formulation of objective function for optimum regulation of dc-link voltage using a BFO-based optimized PI controller. Investigations are carried out under identical test environments for ideal, distorted and unbalanced supply voltage conditions. Results obtained from rigorous simulations in MATLAB, followed by real-time performance analysis in Opal-RT Lab are presented in section 'Results and discussion'. Finally, the reported work is concluded with important remarks in section 'Conclusion'.

System description

This paper focuses on shunt APF for compensation of harmonics and reactive power. Fig. 1 shows the system configuration of shunt APF employing cascaded m-level MLI. Voltages in three phases of supply is presented by (V_{sa}, V_{sb}, V_{sc}). Nonlinear load (diode rectifier with RL load on its dc side) connected to the system draw non-sinusoidal nature of current (i_{La}, i_{Lb}, i_{Lc}). In the absence of APF, current drawn from utility (i_{sa}, i_{sb}, i_{sc}) is exactly same as the load current i.e.

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{1}$$

Compensation current generated by the APF is of exactly same magnitude but 180° out of phase as the harmonics in load current. The APF is connected to power system through a small RL filter (R_c, L_c) at the PCC, to inject filter current (i_{ca}, i_{cb}, i_{cc}) so as to make the resultant source current sinusoidal, i.e.

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} + \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} \tag{2}$$

To suppress the additional undesirable high frequency current harmonics generated by the power converter during switching action of power electronic devices, a small filter inductor (R_c, L_c) is used. This prevents the other sensitive loads present on the common utility grid from getting disturbed [27,28]. Using a large filter inductor will result in a huge power loss, more heat dissipation,