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A new dual bridge multilevel dc-link inverter topology

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ABSTRACT

This paper attempts to construct a new hybrid multilevel dc-link inverter (MLDCLI) topology with a focus to synthesize a higher quality sinusoidal output voltage. The idea emphasizes the need to reduce the switch count considerably and thereby claim its superiority over the existing multilevel inverter (MLI) configurations. The structure incorporates a new module along with a differently used H-bridge that facilitates the increase in levels with much lower switch counts. The proposed dual bridge MLDCLI (DBMLDCLI) is evaluated using phase disposition (PD) multi-carrier pulse width modulation (MC-PWM) strategy in a filed programmable gate array (FPGA) platform. The MATLAB/System generator based simulation results validated through FPGA based prototype for a typical output level exhibit the drastic enhancement in the quality of output voltage. The total harmonic distortion (THD) obtained using a harmonic spectrum reveals the mitigation of the frequency components of output voltage other than the fundamental and paves the way to open a new avenue for nurturing innovative applications in this domain.

1. Introduction

MLIs are preferred for high power medium voltage applications owing allegiance to their inheritance of reduced harmonic content in the output side, lower blocking voltage in the switching devices and diminished losses due to less commutation stresses [1–8]. They appear to be an attractive solution for high power drives and reactive power compensation applications due to their ability to offer higher voltages from medium voltage dc-link and less distorted output voltage [9–17].

The introduction of a MLDCLI structure [18] invades far reaching consequences to orient an improved performance. It groups itself in either of the categories neutral point clamped phase leg [1,19], flying capacitor phase leg [20,21] or cascaded half bridge cells [22] with each cell having its own dc sources. These inverters reduce the number of switches and gate drivers as the number of voltage level increases. However, they evince inconveniences in their operation with balancing capacitor voltages [5,23]. A new variety of MLDCLI coined as series parallel switched multilevel dc-link inverter (SPSMLDCLI) synthesizes a nearly distortion less sinusoidal output voltage which uses lower number of sources, power switches and eliminates the necessity of capacitors [24].

It is in this direction that there is a charter to develop a new class of MLDCLI topology namely dual bridge multilevel dc link inverter (DBMLDCLI) which requires a lower switch count to obtain a nearly sinusoidal voltage. The structure incorporates a module along with a differently used H-bridge that facilitates the increase in levels in addition to another H-bridge which account for the bi-directional power flow. The proposed DBMLDCLI is evaluated both using simulation and a suitable prototype. It seeks the role of phase disposition (PD) multi-carrier pulse width modulation (MC-PWM) strategy implemented using a Xilinx based system generator facility available as a toolbox in MATLAB R2010a in conjunction with a FPGA based processor [25].

2. Proposed topology

A MLDCLI in its very generic form shown in Fig. 1 is constituted of two H-bridges and a number of distinctive modules depending on the level requirements. It depicts the general configuration of the proposed MLDCLI structure coined as DBMLDCLI through which it is viable to realize as many desired levels. While the modules and the first H-bridge serve to increase the level of the dc-link voltage, the second H-bridge provides bi-directional power flow through the load. The first bridge is connected in series with as many modules for every six level increase, with each module intertwined with a switch in series with the source, the combination shunted through an anti parallel diode. The precise number of

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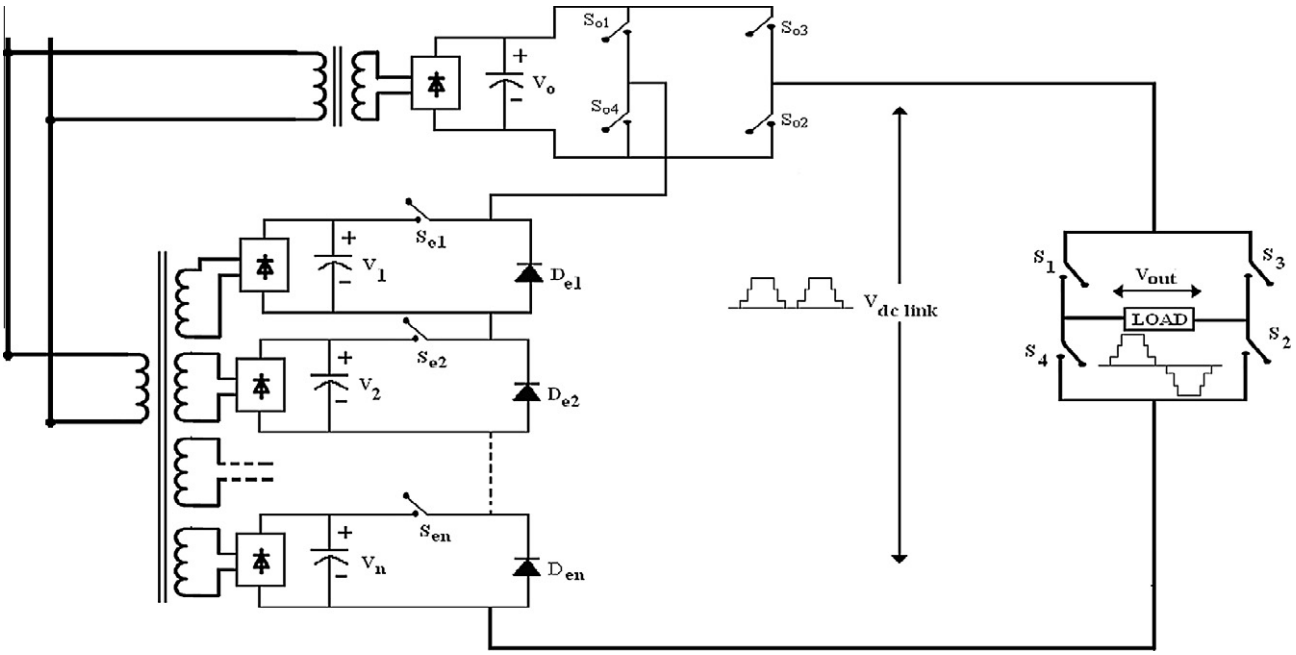

Fig. 1. Generalized structure of DBMLDCLI.

Table 1
Comparison between topologies for 15 level.

Multilevel inverter structure	Cascaded H-bridge	Diode clamped	Flying capacitor	Multilevel dc-link inverter			Proposed topology
				Cascaded half bridge	Diode clamped	Flying capacitor	
Main switches	28	28	28	18	18	18	10
Bypass diodes	–	–	–	–	–	–	2
Clamping diodes	–	24	–	–	12	–	–
DC split capacitors	–	6	6	–	6	6	–
Clamping capacitors	–	–	12	–	–	6	–
DC sources	7	1	1	7	1	1	3
Total	35	59	47	25	37	31	15

Table 2
Comparison in terms of power components used for different level.

No. of Levels	No. of power switches		No. of bypass diodes	
	SPSMLDCLI	DBMLDCLI	SPSMLDCLI	DBMLDCLI
15	10	10	1	2
21	13	11	1	3
27	16	12	1	4
33	19	13	1	5
39	22	14	1	6

levels of output voltage that a DBMLDCLI can synthesize is expressed using a relation $(2(3n + 1) + 1)$ where n is the number of voltage sources excluding V_0, if arranged in the ratio $V_0{:}V_n = 1{:}3$. It contributes to decreasing the switching losses, increasing the efficiency and eliminating the consequent effects of de-rating.

A detailed comparison of the switch and source requirements is tabulated in Table 1 to bring out the reduction in the count that the proposed DBMLDCLI enjoys over the existing MLI topologies for a typical case of fifteen level output. Table 2 narrates comparison

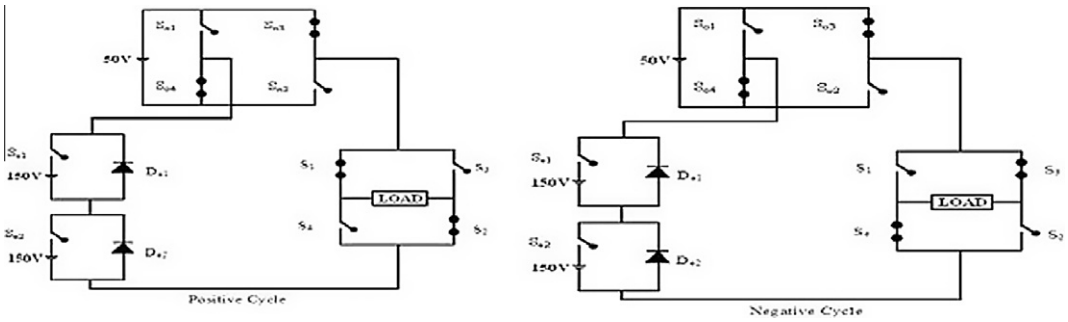

Fig. 2. DBMLDCLI operating mode-level 1 (±50 V).