Electrical Power and Energy Systems 83 (2016) 7–14

Contents lists available at ScienceDirect

Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes

Enhanced high-speed electromagnetic transient simulation of MMC-MTdc grid

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ARTICLE INFO

Article history:
Received 4 October 2015
Received in revised form 21 March 2016
Accepted 29 March 2016
Available online 12 April 2016

Keywords:
Thévenin equivalent
Backward Euler (BE) method
Modular multilevel converter (MMC)
Nearest level control (NLC)
MMC-MTdc grid

ABSTRACT

This paper introduces a very fast electromagnetic transient (EMT) simulation model for the HVdc modular multilevel converter (MMC) that maintains the identity of each switching level, but achieves computation speeds comparable to the much simplified averaged-value models (AVMs) when simulating the multi-terminal dc grid. Speedup is achieved by representing the off state of a MMC sub-module (SM) with ideal zero conductance, and representing the converter with a companion model using the A-stable Backward Euler (BE) method. Often, the user may wish to use the nearest level control (NLC) based voltage balancing algorithm. Then additional speedup can be obtained by using an efficient sorting algorithm which is integrated into the Thévenin equivalent circuit. This achieves a linear speedup (i.e. order O(N)) with system size. When compared with a fully detailed simulation (no simplifications), the method shows one to two orders of magnitude speed improvement with earlier reported fast MMC models, with negligible loss in accuracy.

Introduction

Modular multilevel converter (MMC) based high voltage direct current (MMC-HVdc) transmission is gaining in popularity as a dc power transmission option with low losses [1–4]. Compared to the conventional 2 and 3-level voltage source converters (VSC), the MMC topology offers several advantages such as:

- Its modular design permits easier scalability to any desired voltage level simply by using more sub-modules (SM)
- The output voltage waveform has negligible ripple content which eliminates the need for ac filters
- No common dc link capacitor is required
- It has lower switching losses and hence high efficiency

In the future, simulation of large scale multi-terminal dc grid with multiple MMCs will be urgently required especially on the off-line electromagnetic transient (EMT) simulation platforms [5]. Novel MMC models have been proposed that approach the accuracy of the detailed MMC model, but greatly reduce the computational effort. These models can be classified into two categories [6]. In the first category [7,8], each SM retains its individual identity, permitting access to its calculated internal voltages and currents. In the second category [9], all the SMs are combined into a single equivalent, accessing to internal capacitor voltages and currents in individual modules is lost and only the external behaviors are preserved.

The model proposed in this paper is of the first category, in that it maintains the individual identity of SMs and approaches the accuracy of fully detailed simulation. However, as it uses idealized representations of the switches (i.e. IGBTs and diodes) and restructuring of the way in which capacitor balancing is simulated. This accelerates the computation speed by an additional 1–2 orders of magnitude over existing high speed first category models and hence approaches the speeds possible with the second category models.

Background: thévenin equivalent MMC model

This section discusses relevant previous work on developing a faster MMC model [8]. Later sections will show how this is extended to construct the even faster models which are the contributions of this paper. The fully detailed MMC model is comprised of three phase legs and each leg consists of two phase arms, as shown in Fig. 1.

Each phase arm includes N identical SMs and a reactor L_S, I_{ARM} indicates the arm current. The SM is the basic building block of

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http://dx.doi.org/10.1016/j.ijepes.2016.03.062
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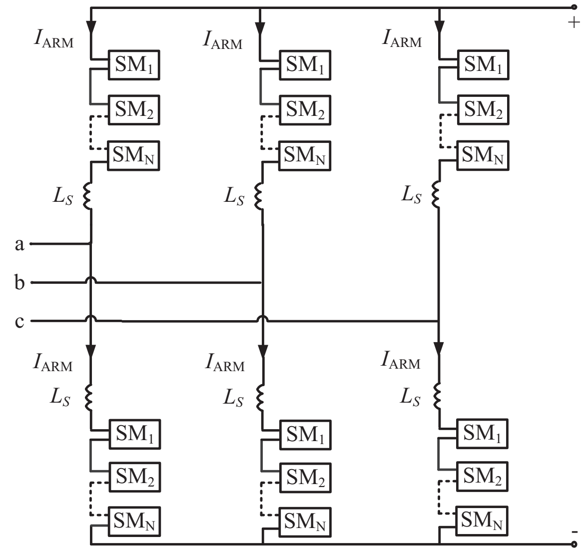

Fig. 1. Schematic diagram of three-phase MMC.

MMC, as shown in Fig. 2(a). It consists of an insulated gate bipolar transistor (IGBT) half-bridge (IGBTs T1, T2 and diodes D1, D2) and a dc storage capacitor *C*.

Each IGBT switch (i.e. the parallel connection of an IGBT and a diode) in Fig. 2(a) can be treated as two-state resistive devices [10]. In Fig. 2(a)–(c), I_{SM} equals to I_{ARM} as in Fig. 1.

Using the Trapezoidal Rule (TR), a companion circuit is constructed as shown in Fig. 2(b). The resistance and voltage source values as functions of time are given by (1) and (2). Capacitor current $I_C(t)$ in Fig. 2 is obtained as (3), in which I_{ARM} represents the arm current. The superscript "T" indicates that TR was used in the construction of the companion model.

$$R_C^T = \frac{\Delta T}{2C} \tag{1}$$

$$V_{CEQ}^T(t-\Delta T) = V_C^T(t-\Delta T) + R_C^T I_C(t-\Delta T) \tag{2}$$

$$I_C(t) = \frac{I_{ARM}(t)\cdot R_2 - V_{CEQ}(t-\Delta T)}{R_1+R_2+R_C} \tag{3}$$

Using TR, the updated capacitor voltage at time *t* can be obtained from the voltage at time $(t-\Delta T)$ as in (4):

$$V_C^T(t) = V_C^T(t-\Delta T) + \Delta V_C^T \tag{4a}$$

$$\Delta V_C^T(t) = [I_C(t-\Delta T) + I_C(t)] \times R_C^T \tag{4b}$$

Converting Fig. 2(b) into a Thévenin equivalent gives the circuit of Fig 2(c), with the equivalent parameters R_{SMEQ} and V_{SMEQ} given by (5) and (6).

$$R_{SMEQ}(t) = R_2 \times \left(1 - \frac{R_2}{R_1+R_2+R_C}\right) \tag{5}$$

$$V_{SMEQ}(t-\Delta T) = \left(\frac{R_2}{R_1+R_2+R_C}\right) \times V_{CEQ}(t-\Delta T) \tag{6}$$

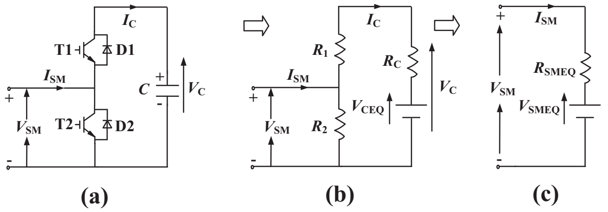

Fig. 2. Schematic diagram of MMC SM: (a) electric circuit, (b) companion equivalent circuit (c) SM Thévenin equivalent.

The Thévenin equivalents of the *N* SMs in the bridge arm are then compressed into a single Thévenin equivalent as shown in the dashed area of Fig. 3.

In normal operation, the ON/OFF states of the SMs are determined by the controllers, V_C and T_{SM} in Fig. 3 are the output capacitor voltages and input firing pulses of the SMs. The values of the Thévenin equivalent resistance R_{ARMEQ} and the equivalent voltage V_{ARMEQ} are given by (7) and (8) where V_{SMEQ_i} and R_{SMEQ_i} are the Thévenin voltage and resistance of the *i*th SM as in Fig. 2(c).

$$R_{ARMEQ}(t) = \sum_{i=1}^{N} R_{SMEQ\_i}(t) \tag{7}$$

$$V_{ARMEQ}(t-\Delta T) = \sum_{i=1}^{N} V_{SMEQ\_i}(t-\Delta T) \tag{8}$$

However, this is not the case when the MMC valves are blocked, which occurs during MMC startup, protective actions, etc. When all the IGBTs are blocked the arms are only affected by the diodes, which determine whether the SMs are bypassed or inserted simultaneously, depending on the arm current directions.

In block state, the MMC arm can be modeled using the circuit shown in Fig. 3 [5], the two diodes D1 and D2 are used to represent the current direction selection effects. And the breakers BRK_1 and BRK_2 are responsible for changing the working modes of MMC either in normal operation or blocking state. If I_{ARM} is positive, the Thévenin equivalent resistance R_{ARMEQ} and voltage V_{ARMEQ} are used to represent the diodes and capacitors in Fig. 2, which can be respectively obtained from (7) and (8) through assuming all the SMs are inserted. If I_{ARM} is negative, the resistance R_{ON_EQ} is used to represent the conducting resistance of the diodes in Fig. 2, which can be calculated using (9).

$$R_{ON\_EQ} = N \cdot R_{ON} \tag{9}$$

Regarding the equivalent circuit of MMC, no detail is lost in this process, but the overall final representation in the EMT solver is very simple, which leads to a much faster solution. However, even though this approach results in up to two orders of magnitude saving in computation time [8], it is still much slower than the less accurate AVMs [9], and hence modeling multi-terminal dc grids with several MMCs can still take a long time. The next section discusses the principal contributions of this paper, which is an attempt to further speed up the computation speed by another 1 or 2 orders of magnitude, without significant loss of accuracy.

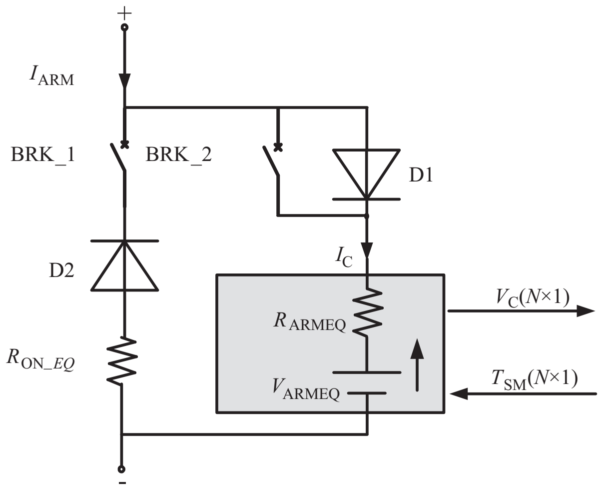

Fig. 3. Thévenin equivalent for a single phase arm of MMC under both normal and blocking states.