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A generalized analog implementation of piecewise linear neuron models using CCII building blocks

Hamid Soleimani [a], Arash Ahmadi [a,*], Mohammad Bavandpour [b], Ozra Sharifipoor [a]

[a] Electrical Engineering Department, Razi University, Kermanshah, Iran

[b] Faculty of Electrical Engineering, Sharif University of Technology, Tehran, Iran

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ABSTRACT

This paper presents a set of reconfigurable analog implementations of piecewise linear spiking neuron models using second generation current conveyor (CCII) building blocks. With the same topology and circuit elements, without W/L modification which is impossible after circuit fabrication, these circuits can produce different behaviors, similar to the biological neurons, both for a single neuron as well as a network of neurons just by tuning reference current and voltage sources. The models are investigated, in terms of analog implementation feasibility and costs, targeting large scale hardware implementations. Results show that, in order to gain the best performance, area and accuracy; these models can be compromised. Simulation results are presented for different neuron behaviors with CMOS 350 nm technology.

1. Introduction

Spiking neural networks (SNNs) have received considerable attention and an increasing research interest in developing artificial neural networks during the past few years (Gerstner & Kistler, 2002; Hodgkin & Huxley, 1952; Izhikevich, 2001, 2003, 2007), due to their behavioral resemblance to biological neurons. Motivated by biological discoveries, pulse-coupled neural networks with spike-timing are considered as an essential component in biological information processing systems, such as the implementation of both high-level and low-level features of the brain like performing complex pattern recognition, motor control, autonomous learning, adaptability, robustness against noise and fault tolerance. Implementation of these models, targeting different platforms, has been the subject of studies in terms of efficiency and large scale simulations (Andreou, Meitzler, Strohbehn, & Boahen, 1995; Arthur & Boahen, 2011; Camuñas-Mesa, Acosta-Jiménez, Zamarreño-Ramos, Serrano-Gotarredona, & Linares-Barranco, 2011; Davies, Galluppi, Rast, & Furber, 2012; Indiveri, Chicca, & Douglas, 2006; Serrano-Gotarredona, Serrano-Gotarredona, Acosta-Jiménez, & Linares-Barranco, 2006; Sharifipour & Ahmadi, 2012; Soleimani, Ahmadi, & Bavandpour, 2012; van Schaik, 2001; Wijekoon & Dudek, 2008; Yamashita & Torikai, 2012). Although digitally implemented simulators are found to be convenient and practical for behavioral study of neural networks, they are not suitable for actual biologically plausible systems, or detailed real-time and large-scale simulations of neural systems. Custom digital systems that exploit parallel graphical processing units (GPUs) (Ahmadi & Soleimani, 2011) or field programmable gate arrays (FPGAs) (Soleimani et al., 2012) may offer such capabilities in future, but it is not clear how such systems could be able to approach the density, energy efficiency and resilience of the neurons and synapses which they model.

The observation that the brain operates based on analog principles of the physics of neural computation that are fundamentally different from digital principles in traditional computing, has initiated the investigations in the field of analog implementation of neuro-systems. Motivated by these reasons, utilizing well developed electronic components and analog circuits to mimic neurological behaviors, is considered as the main choice for direct implementation of neuro-systems. If one can provide a suitable reconfigurable platform to implement neural structures, very large scale integration (VLSI) implementation can be used for prototyping of the neural models, neural dynamics, network structures, and learning mechanisms to test different theories. In terms of VLSI implementation, analog implementations can replicate neural dynamics down to the ion channels in the neural membrane and are fast and efficient; but they are inflexible and require a long development time. As a midpoint in the design space, reconfigurable platforms can provide compact and flexible solutions for biologically plausible neuro-system designers.

Many different neuron models are described by nonlinear Ordinary Differential Equations (ODEs) such as the Hodgkin–Huxley model (Hodgkin & Huxley, 1952) or nonlinear ODEs with

* Corresponding author. Tel.: +98 8314283261; fax: +98 8314283261.
E-mail addresses: aahmadi70@gmail.com, aahmadi70@yahoo.com (A. Ahmadi).

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state-dependent resets (Gerstner & Kistler, 2002; Izhikevich, 2001, 2003, 2007). These models are based on the bio-chemical inspection of the neuron structure and mostly are expressed in the form of differential equations. Although detailed neuron models (Hodgkin & Huxley, 1952), can imitate most experimental measurements to a high degree of accuracy, they are mostly complicated and difficult to physically implement. Izhikevich (2003), has developed a class of models for spiking neurons, which balances the computational efficiency of integrate and fire (IF) models with the biological plausibility and versatility of Hodgkin–Huxley type models (Hodgkin & Huxley, 1952).

An analog circuit for implementation of the Izhikevich neuron model has been reported in the literature (Wijekoon & Dudek, 2008). Although this model cannot exactly implement the standard neuron model responses (Izhikevich, 2003), it allows the implementation of some cortical neuron behaviors. The spiking shapes produced by the circuit are biologically plausible and some of the spiking patterns can be obtained by changing two out of the four parameters in the neuron model (V_c and V_d). The circuit has a low reconfigurability, because the variable parameters after implementation are only two out of the four and the other parameters are fixed.

Recently, a novel reconfigurable analog circuit implementation of the neuron has been presented using a second generation current conveyor (CCII) (Sharifipour & Ahmadi, 2012). This circuit is based on a new piecewise linear (PWL) modification of the Izhikevich model, which can reproduce different dynamic behaviors of the cortical neurons. Due to the regular structure of the circuit using standard building blocks, it has the capability to be realized as an application specific reconfigurable analog device, targeting neural networks. This can be considered as a step towards programmable analog neural integrated circuits. Moreover, the resistant structure against noise and impedance matching in the input and output, make this model a suitable choice for analog implementation of large scale neural networks. In this paper, a generalized analog implementation of piecewise linear neuron models consisting of implementation of third and fourth piecewise linear models using reconfigurable CCII building blocks is proposed.

2. The PWL spiking neuron models

In Izhikevich (2003) proposed a model of two coupled differential equations as:

$$\begin{cases} \dfrac{dv}{dt} = 0.04v^2 + 5v + 140 - u + I \\ \dfrac{du}{dt} = a(bv - u) \end{cases} \tag{1}$$

with the auxiliary reset equations:

$$v \geq 30\ \text{mV} \quad \text{then} \begin{cases} v \leftarrow c \\ u \leftarrow u + d \end{cases} \tag{2}$$

where v represents the membrane potential of the neuron, u represents a membrane recovery variable, which accounts for the activation of K^+ ionic currents and inactivation of Na^+ ionic currents and it provides negative feedback to v. Parameters a, b, c, d are constant values, describing neuron type. After the spike reaches its apex (30 mV), the membrane voltage and the recovery variable are reset according to the equations above. To improve the computational efficiency of the Izhikevich model, three piecewise linear approximations have been proposed in Soleimani et al. (2012).

2.1. Second order piecewise linear model

The second order piecewise (2PWL) model approximates the quadratic part of the Izhikevich model with two crossed lines. This approximation can be formulated as:

$$\begin{cases} \dfrac{dv}{dt} = k_1|v + k_2| - k_3 - u + I \\ \dfrac{du}{dt} = a(bv - u). \end{cases} \tag{3}$$

This approximation provides three degrees of freedom to achieve the closest behavior to the original model.

2.2. Third order piecewise linear model

For the third order piecewise (3PWL) approximation the following function is presented:

$$\begin{cases} \dfrac{dv}{dt} = k_1(|v + k_2| + |v - k_2|) - k_3 - u + I \\ \dfrac{du}{dt} = a(bv - u). \end{cases} \tag{4}$$

This approximation provides three degrees of freedom to achieve the closest behavior to the original model. In terms of implementation, the 3PWL approximation is more expensive compared to the 2PWL, but the behavior of the 3PWL model can be closer to the original model by appropriate choice of the coefficients.

2.3. Fourth order piecewise linear model

The proposed fourth order piecewise (4PWL) approximation is formulated as:

$$\begin{cases} \dfrac{dv}{dt} = k_2(|v + k_3| + |v - k_3|) + k_1|v + k_4| - k_5 - u + I \\ \dfrac{du}{dt} = a(bv - u) \end{cases} \tag{5}$$

where k_1, k_2, k_3, k_4, k_5 similar to the other PWL models, are constant values. This approximation provides five degrees of freedom for achieving the closest behavior to the original model. This model requires more complex circuit implementation compared to the other PWL models, but has a very close behavior compared to the other models.

3. Bifurcation analysis of PWL models

This section investigates the qualitative bifurcation analysis of the 2 and 4PWL neuron models and explains their relations to a standard biological neuron model (Izhikevich, 2003) based on the procedure introduced in Yamashita and Torikai (2012). Due to similarity of the analyses across all three models, as a midpoint we have waived the analysis of the 3PWL model.

3.1. Basic neuron responses

Resting states: The eigenvalues of the PWL dynamical systems have a negative real part, called the *nodal sink*, in the states of Fig. 1(a1–a2) therefore the intersection point of the borders attracts any nearby point. This phenomenon is also referred to as a *stable resting state* (Izhikevich, 2003). Moreover, if both eigenvalues have positive real part, the intersection point repels any nearby point named *nodal source* in Fig. 1(b1–b2). Such a phenomenon is known as an *unstable resting state*.