An analog implementation of biologically plausible neurons using CCII building blocks

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ARTICLE INFO

ABSTRACT

This study presents an analog implementation of the spiking neurons based on a piecewise-linear model. This model is a variation of the Izhikevich model, which is capable of reproducing different dynamic behaviors. The proposed circuit utilizes second generation current conveyors (CCII) building blocks. With the same topology and circuit values, this circuit can produce a wide variety of neuron behaviors just by tuning the reference current and voltage sources. In addition, since CCII can be considered as a building block for programmable analog arrays, based on the proposed circuit different neuron types can be implemented on programmable analog platforms. Simulation results are presented for different neuron behaviors with CMOS 350 nm ±1.5 V technology using HSPICE.

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1. Introduction

Modeling and implementation of bio-inspired computing circuits and systems are important because of two main reasons. The first is exploring new computational paradigms to enrich or go beyond the standard computation models and architectures. The second is to provide more accurate tools and devices for biological system studies. Motivated by both reasons, neural systems, as the most powerful natural computers, have been the subject of research efforts ranging from mathematics to biology for decades. Among all the possibilities, VLSI, by utilizing well developed electronic components and circuits to mimic neurological behaviors, is considered as the main choice for direct implementation of the neuro-systems. If one can provide a suitable reconfigurable platform to implement neural structures, VLSI implementation can be used for rapid prototyping of the neural models, neural dynamics, network structures, learning mechanisms and algorithms to test different theories with minimum effort. In terms of VLSI implementation, a variety of analog and digital implementations of spiking neural networks have been presented. While analog implementations can replicate neural dynamics down to the ion channels in the neural membrane and are fast and efficient, they are inflexible and require a long development time (Folowosele et al., 2009; Renaud, Tomas, Bornat, Daouzli, & Saighi, 2007; Simoni & DeWeerth, 1999; Wijekoon & Dudek, 2008). On the other hand digitally implemented

neurobiological systems are flexible, however they are often large, computationally slow, and power consuming if implemented using general purpose systems (Blue Brain Project, 2011; BRAINSCALES project, 2011; IFAT 4G project, 2011; Jin, Lujan, Plana, & Davies, 2010; Neurogrid project, 2011). As a midpoint in the design space, reconfigurable platforms can provide compact and flexible solutions to biologically plausible neuro-system designers.

Many different models have been presented for spiking neural networks to reproduce their dynamical behavior. These models are based on the bio-chemical inspection of the neuron structure and mostly are expressed in the form of differential equations. Although detailed neuron models, (Hodgkin & Huxley, 1952), can imitate most experimental measurements to a high degree of accuracy such as Hodgkin–Huxley, they are difficult to be used in large scale artificial spiking neural networks, due to their complexity (Gerstner & Kistler, 2002). Consequently, simplified models are highly popular for studies of neural information coding, memory and network dynamics. Lapicque, (Brunel & van Rossum, 2007), proposed that spikes are generated when the integrated sensory or synaptic input to a neuron reaches a threshold value; this model is called Integrate and Fire (IF). IF has become one of the most influential models in neuro-computing giving a simple explanation for the basic neural operations. Advances in experimental techniques have shown, however, that the IF model is far from accurate in describing real neurons. Izhikevich, (Izhikevich, 2003), has developed a class of models for spiking neurons which balances the computational efficiency of IF models with the biological plausibility and versatility of Hodgkin–Huxley type models (Hodgkin & Huxley, 1952).

This paper is based on a new piece-wise linear (PWL) modification of the Izhikevich model (Ahmadi & Zwolinski, 2010), which is efficiently implementable in analog schemes, yet

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accurate with a behavior similar to the original model. Based on this piece-wise linear model, a novel reconfigurable analog circuit implementation of the neurons is presented using second generation Current Conveyor (CCII), which can reproduce different dynamic behaviors of the cortical neurons. Due to the regular structure of the proposed circuit using standard building blocks, it has the capability to be realized on reconfigurable analog devices. This can be considered as a step towards programmable analog neural integrated circuits.

The paper is organized as follows. Section 2 introduces the modified model while a short explanation of CCII as the building block is presented in Section 3. The circuit implementation of the model and its simulation results are presented in Sections 4 and 5 respectively and the paper is concluded in Section 6.

2. The proposed PWL neuron Mmdel

In Izhikevich (2003) Izhikevich proposed a model of two coupled differential equations as:

$$\begin{cases} \dfrac{dv}{dt} = 0.04v^2 + 5v + 140 - u + I(t) \\ \dfrac{du}{dt} = a(bv - u) \end{cases} \quad (1)$$

with the auxiliary after-spike resting equations:

$$v \geq V_{\text{th}} \quad \text{then} \quad \begin{cases} v \leftarrow c \\ u \leftarrow u + d \end{cases} \quad (2)$$

where a, b, c and d are constant values, describing neuron type, $I(t)$ is the input current, v represents the membrane potential of the neuron and u represents the membrane recovery variable. In this model u accounts for the activation of K^+ ionic currents and inactivation of Na^+ ionic currents, providing a negative feedback to v. After the spike reaches its apex (Vth), the membrane voltage and the recovery variable are reset according to Eq. (2). If v skips over Vth, then it first resets to Vth and then to c so that all the spikes have equal magnitudes. The part $0.04v^2 + 5v + 140$ is chosen so that v is in mV scale and time is in ms. In steady state (without input), the Izhikevich model is:

$$\begin{cases} u = 0.04v^2 + 5v + 140 \\ u = bv. \end{cases} \quad (3)$$

Geometrically, these equations represent a parabolic curve and a line, as depicted in Fig. 1. The crossing points of the curves give the equilibrium points of the system (neuron). Different spiking patterns are produced by changing these crossing points and the threshold action potential. Although this model is known as the most practical, yet accurate, available model, still there are several challenges in realizing the model using analog circuits. To improve the realization efficiency of the model, a piecewise linear replacement for the quadratic part in the equation is proposed in Ahmadi and Zwolinski (2010) as:

$$\begin{cases} \dfrac{dv}{dt} = k_1|v - k_2| + k_3 - u + I \\ \dfrac{du}{dt} = a(bv - u) \end{cases} \quad (4)$$

where k_1, k_2 and k_3 are constant values satisfying:

$$\begin{cases} 12.5\left((b-5) - \sqrt{b^2 - 10b + 2.6}\right) = \dfrac{k_3 - k_1 k_2}{b - k_1} \\ 12.5\left((b-5) + \sqrt{b^2 - 10b + 2.6}\right) = \dfrac{k_3 + k_1 k_2}{b + k_1}. \end{cases} \quad (5)$$
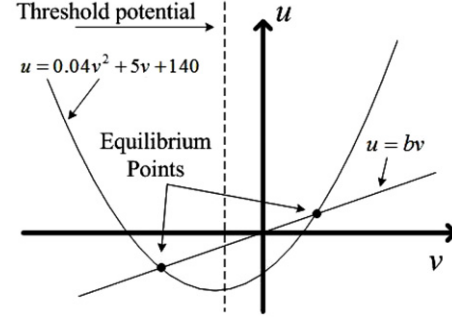

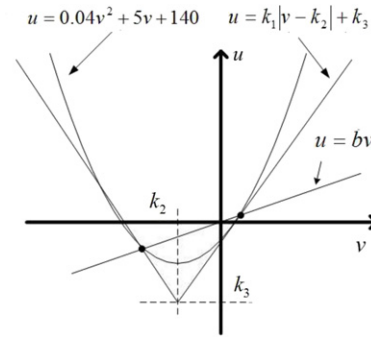
Fig. 1. Equilibrium locus of the Izhikevich model.

Fig. 2. Piecewise-linear approximation of the second order part of the model.

This piecewise linear model is depicted in Fig. 2 together with the original model. As it is attainable from Fig. 2, this approximation provides three degree of freedom to achieve the closest behavior to the original model. A more detailed explanation and verification of the model can be found in Ahmadi and Zwolinski (2010).

3. Second generation current conveyor

In general, current mode analog circuit design is attractive because of wide bandwidth, low power consumption, high slew rate and simple circuitry. The second generation current conveyor (CCII), (Sedra & Smith, 1970), is one of the most versatile current mode building blocks analogous to an operational amplifier in the voltage mode circuit design. Because of their wide bandwidth and low power consumption, the current conveyor continues to attract more attention in analog design (Dutta, Serdijn, Banerjee, & Gupta, 2005; Elwan & Soliman, 1996; Elzahar, Elwan, & Ismail, 2003; Gaudet & Gulak, 1997; Grigorescu, 2008; Hwang, Liu, Tu, & Chin, 2009; Priemont, Grisel, Abouchi, & Chante, 1998). CCII in conjunction with other components can implement several basic analog functions such as integrator, amplifier, multiplier, filter and many other signal processing operations. This generality has made them a serious candidate for programmable analog arrays (Gaudet & Gulak, 1997; Priemont et al., 1998).

The operational model of the CCII± is a three port component (namely X, Y and Z terminals) with the matrix representation of the terminal voltages and currents as:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (6)$$

where the positive and negative signs of the current Iz denote the non-inverting CCII1 and inverting CCII2, respectively. The current