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A spiking and bursting neuron circuit based on memristor

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ABSTRACT

In this paper, we propose two emulator circuits. Firstly, we present a novel memristor emulator based on operational transconductance amplifier (OTA) which is different from classical TiO_2 memristor. This memristor emulator has a threshold switching mechanism. Secondly, we create a novel neuron circuit using proposed memristor, which is capable of generating spiking and bursting firing behaviors, with a biologically plausible spike shapes. The behavior of this neuron circuit can be adjusted by changing only one external biasing voltage. This neuron circuit mimics the behavior of cortical neurons, such as regular spiking (RS), intrinsic bursting (IB), chattering (CH) and fast spiking (FS). Proposed emulator circuits are compatible with VLSI systems and they can also be implemented by using discrete circuit components for different applications.

1. Introduction

The brain, composed of billions of billions of neural cells, consumes about 20 W of power. The neurons are also complex and adaptive structures that make connections between each other via synapses. These synapses can change their function dramatically depending upon the spike encoded messages they receive. These changes are thought to provide energy efficiency during signal transmission as well as flexibility to direct the storage and recall of information in the brain [1–4]. To understand how the brain works, we need more numerical and experimental studies of brain models. These models or circuits for biological systems must be simple and capable of producing rich firing patterns.

Many neuron models have been proposed by researchers, some most popular models: Hodgkin–Huxley [5], Integrate and Fire [6], FitzHugh–Nagumo [7], Hindmarsh–Rose [8] and Izhikevich [9]. Prof. Carver Mead pioneered electronic system design and coined the term neuromorphic electronics [10]. Implementation of neural network has attracted increasing research interest [11–21]. The basic components of the brain are neuron cells. Mimicking the neuron cells is a subject of ongoing research field [11,22–27].

Chua [28] postulated the existence of a new two-terminal basic electrical circuit element, called the memristor (a contraction for memory resistor), defined by a constitutive relationship between flux and charge linkage. However, this work [29] had not attracted the researchers' attention until 2008. In 2008, Williams and co-workers from HP Labs published on the experimental design of memristor. After this work, a tremendously increased interest in the field of the theory and applications about the memristor. Commercially available memristors are not expected to appear in the near future due to the cost and technical difficulties in fabricating nano-scale devices [30]. For this reason, a number of SPICE models were developed [31–35], including emulators [30,36–46]. Some of the properties of the memristor can actually be outlined here: 1. Work as a passive element (like a resistor); 2. History dependent (depends on state-variable); 3. Polarized element (current direction cares); 4. Frequency-dependent (time derivative of the state variable). All these properties exist in a synapse! [47].

In this paper, we design a new memristor emulator and a new neuron circuit based on designed memristor. The memristor with hard switching characteristic is designed by showing experimental results, which is different from TiO_2 and other memristor device characteristics. After design and implementation the simple memristor we present simple neuron circuit based on memristor that produces with spiking and bursting firing patterns. The neuron circuit mimics the behavior of cortical neurons: regular spiking (RS), intrinsic bursting (IB), chattering (CH) and fast spiking (FS).

2. Circuit design

2.1. Memristor emulator architecture

Commercially availability of memristor is difficult due to technical reasons. For this reason many memristor emulators were

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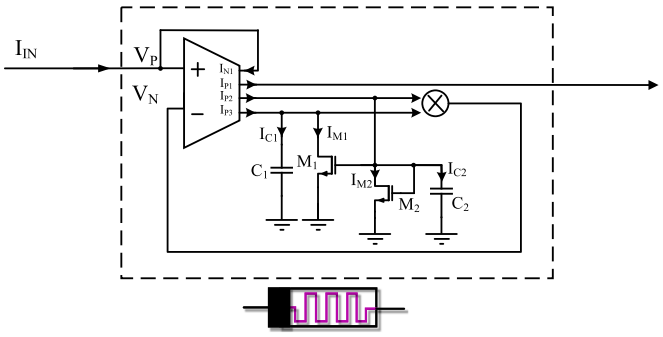

Fig. 1. Memristor emulator based on operational transconductance amplifier (OTA).

designed [31–46]. But many of them emulate TiO_2 memristor. Here we designed a new memristor emulator different from classical HP memristor [29]. Our memristor has hard switching characteristics and similar to Mott memristor [48].

Using the OTA fundamental equation for the circuit given in Fig. 1,

$$I_{IN} = g_m(V_P - V_N) \tag{1}$$

V_N is obtained V_{C1} multiple by V_{C2}.

$$V_N = 0.1 \times V_{C1} \times V_{C2} \tag{2}$$

$$I_{IN} = g_m(V_P - 0.1 \times V_{C1} \times V_{C2}) \tag{3}$$

The input current (I_{IN}) equals to each output current of OTA ($I_{IN} = I_{OUT}$) and for this reason one of the output currents equals to the sum of the currents of capacitor and transistor.

$$I_{OUT} = I_{C1} + I_{M1} \tag{4}$$

Current is integrated on capacitor C_1,

$$C_1 \frac{dV_{C1}}{dt} = I_{OUT} - I_{M1} \tag{5}$$

$$I_{OUT} = I_{C2} + I_{M2} \tag{6}$$

Current is integrated on capacitor C_2,

$$C_2 \frac{dV_{C2}}{dt} = I_{OUT} - I_{M2} \tag{7}$$

The top output (I_{N1}) is used to provide fixed initial part of memristance. The second terminal (I_{P1}) is floating output of the proposed emulator. Two capacitors are charged by the I_{P2} and I_{P3} terminals of OTA when voltage is applied to the memristor emulator circuit. M_1 and M_2 transistors are driven by the voltage of C_2 capacitor. When the voltage of C_2 capacitor becomes greater than the threshold voltages of M_1 and M_2, currents start flow from drain to source of the transistors. Capacitors discharged through the transistors at the same but the voltages of capacitors are different from each other because of the fact that they have different values. If there is no voltage across the memristor, non-volatile characteristics of our emulator can be obtained because of the fact that capacitors cannot discharge through the transistors.

Fig. 1 shows the schematic of the proposed memristor emulator circuit. This emulator is designed for neuron circuits and uses one multi-output operational transconductance amplifier (OTA), two capacitors, two nMOSs and one multiplier.

We have built the memristor emulator with the devices listed in Table 1. The voltages of C_1 and C_2 capacities are multiplied by the voltage multiplier. Multiplication of these two voltages provide hysteresis characteristic of the emulator.

There are various studies about the properties of memory circuit elements [28,49,50]. These elements have frequency-dependent characteristic and hysteresis loop in their constitutive variables when applied a periodic input signal. Hysteresis of elements under periodic input may strongly depend on initial conditions [51]. In addition, at very low frequencies, memory circuit elements behave as non-linear elements while at high frequencies as linear elements. We point out that a distinctive signature of memory devices is a hysteresis loop and frequency-dependent characteristic.

Table 1
Active and passive components of the memristor emulator.

Devices list	
OTA	OPA860
Multiplier	AD633
M_1, M_2	ALD1116PAL
C_1	330 pF
C_2	100 nF

The emulator is very simple, appropriate to VLSI technology and to build on a breadboard with the discrete circuit elements for other applications. The input signals were 1, 3, 12 kHz sinusoidal voltages with 1.2 Vp. Fig. 2 shows oscilloscope displays of voltage–current characteristics measured from the memristor. Operating frequency range of memristor can be tuned by changing C_1 and C_2 values. We can operate the memristor at high frequency range when capacitors values decreased.

2.2. Neuron circuit architecture

We have also built a neuron circuit (Fig. 3) which provides a biologically realistic spike shapes. Memristor is a good candidate for compact neuromorphic implementation. For this reason the required non-linear behavior is obtained using the non-linear mechanism of the memristor. Designed memristor is similar to the Mott memristor characteristic. Pickett and co-workers showed the Mott memristor that exhibit threshold switching, which may not necessarily be memristors [48]. From a technological standpoint, neuron circuits based on Mott memristors are interesting because they switch rapidly (<1 ns) with low transition energy (<100 fJ), scale at least to tens of nanometers, are compatible with conventional front- or back-end complementary metal-oxide-semiconductor materials and processes, and can be fabricated on arbitrary substrates [52]. The neuron circuit introduced here uses one memristor, one capacitor and three transistors. The post-synaptic input current is supplied by an external synapse.

The post synaptic input current is integrated linearly by C_A. The M_A, M_B and M_C are driven by C_A voltage. When the capacitor voltage becomes greater than the threshold voltage of M_A, current start flows from V_{DD} to memristor. M_C transistor acts as a high resistor and drives the M_B transistor. C_A capacitor discharges through M_B transistor. We can tune the V_{GS} and V_{DS} of M_B transistor by changing V_B voltage source.

The current of transistor equations can be used:

$$I_{DS} = 0, \quad \text{when} |V_{GS}| < |V_T| \quad (\text{cut} - \text{off region})$$

$$I_{DS} = \mu C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right) \tag{8}$$

when

$$|V_{GS}| > |V_T| \text{ and } |V_{DS}| < |V_{GS} - V_T| \quad (\text{linear region})$$

$$I_{DS} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$