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# Delay learning architectures for memory and classification

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ABSTRACT

We present a neuromorphic spiking neural network, the DELTRON, that can remember and store patterns by changing the delays of every connection as opposed to modifying the weights. The advantage of this architecture over traditional weight-based ones is simpler hardware implementation without multipliers or digital–analog converters (DACs) as well as being suited to time-based computing. The name is derived due to similarity in the learning rule with an earlier architecture called tempotron. The DELTRON can remember more patterns than other delay-based networks by modifying a few delays to remember the most 'salient' or synchronous part of every spike pattern. We present simulations of memory capacity and classification ability of the DELTRON for different random spatio-temporal spike patterns. The memory capacity for noisy spike patterns and missing spikes is also shown. Finally, we present SPICE simulation results of the core circuits involved in a reconfigurable mixed signal implementation of this architecture.



## 1. Introduction: delay-based learning approach

Neuromorphic systems emulate the behavior of biological nervous systems with the primary aims of providing insight into computations occurring in the brain as well as enabling artificial systems that can operate with human-like intelligence at power efficiencies close to biological systems. Though initial efforts were mostly limited to sensory systems [1,2], the focus of research has slowly shifted towards the implementation of functions of higher brain regions like recognition, attention, classification, etc. However, most of the previous researchers have primarily focused on the implementations of somatic nonlinearity, compact learning synapses and address event representation (AER) for asynchronous communication [3–9]. As a result, there is a need for modeling and understanding the computational properties of other components of our neurons: the axons and dendrites which have been largely ignored till now. This is also facilitated by recent experimental and computational work which has shed light on possible computational roles of these structures.

The research on spiking neural networks has led to the emergence of a new paradigm in neural networks, which has garnered a lot of interest lately. Several recent studies have presented spiking neural networks to implement biologically consistent neural and synaptic mechanisms [10–12]. As shown by Izhikevich, spiking neural networks with axonal delays have immense information capacity [13]. These networks can exhibit a large number of stereotypical spatio-temporal firing patterns through a combination of spike timing dependent plasticity (STDP) and axonal propagation delays. Learning schemes based on modifying delays can be utilized to read out these firing patterns. This has spurred a renewed interest in the possible role of delays and has even led to analog VLSI implementations of delay models of axons [14,15]. In this paper we present a computational model, DELTRON, which can learn spatio-temporal spike patterns by modifying the delay associated with the spikes arriving at a synaptic afferent. Compared to most earlier implementations [14,15] that need '*N*' delay storage elements to memorize a single '*N*' dimensional pattern, we show much increased memory capacity by modifying only a few delays to memorize the most 'salient' part of each pattern. Here 'salient' refers to that part of a spatio-temporal pattern which has maximum synchrony or the largest number of coincidental spikes when observed at the soma of the post-synaptic neuron. The synchronous activity of the neurons has been linked to a variety of cognitive functions. Therefore, delay adaptation, which utilizes the synchrony in spike patterns, can play a role in object recognition, attention and neuronal communication.

In the past, several delay learning schemes have been presented for non-spiking networks [16–18] and some of them have been used in applications like word recognition [19]. In the context of spiking neurons and pulse coupled networks, delay adaptation

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was implemented in [20,21] for biologically motivated networks using standard analog hardware elements. The delay learning rule for recognizing impulse patterns is similar to our method except that in these studies, the delay parameters are adjusted until all the impulses are coincident while we modify only a subset of delays corresponding to the most synchronous spikes. Our learning rule, initially presented in [22], is similar to the one presented in [23] with two differences: we do not have the nonlinear membrane voltage dependent weighting term and we use a single time-based delay adjustment instead of an integral over a time period. More importantly, there is no discussion on the memory capacity of such networks in [23] with the authors having demonstrated the memorization of a single pattern only.

This paper is organized as follows: introduction to delay-based learning approaches is given after which, Section 1 presents the computational architecture of DELTRON followed by the learning algorithm in Section 2. Section 4 presents simulation results. We discuss details of an efficient mixed-signal VLSI implementation of this algorithm in Section 5 and follow it with conclusions in Section 6.

## 2. The DELTRON model

### 2.1. Network architecture

Fig. 1 depicts the architecture of the DELTRON that comprises an integrate and fire (I&F) neuron at the output and $N$ excitatory synapses that receive spiking inputs. Each of these incoming spikes create a delayed excitatory post-synaptic potential (EPSP) that gets linearly summed at the soma. In the bio-physical world, such delays could be attributed to synaptic processes [23] or dendritic propagation times [24]. If the summed membrane potential crosses a threshold, $V_{thr}$, the I&F neuron generates a spike and resets the membrane voltage [25]. We want to develop a learning rule that can modify the delays associated with each input so that only a certain desired set of $P$ patterns can fire the neuron by making the membrane potential cross the threshold.

In this paper, we consider applying the DELTRON to classifying or memorizing patterns in the case where there is exactly one spike on each input $i$ at a random time $x_i$ within a fixed time period $T$, i.e. $x_i \in [1\ \ T]$, $i = 1, 2, \ldots, N$. This case corresponds to applying the DELTRON to classify signals coming from a sensor employing time-to-first-spike (TTFS) encoding [26–28]. Time based encoding is becoming popular recently due to the reduced supply voltage (leading to lower voltage headroom) and increased speeds (leading to higher temporal resolution) in today's deeply scaled VLSI processes; hence, the DELTRON will be very useful as a back end processor for all such temporal encoding sensory systems. Formally, we can express the membrane voltage $V(t)$ as a sum of the EPSPs generated by all incoming spikes as

$$V(t) = \sum_i K(t - t_i) \tag{1}$$

where $K : R \rightarrow R$ is the EPSP kernel function, $d_i$ is the delay of the $i$-th branch and $t_i = x_i + d_i$, $i = 1, 2, \ldots, N$. The vector $\mathbf{x} = (x_1, x_2, \ldots, x_N)$ constitutes a spike pattern presented to the network. In this work, we consider the fast rising and slowly decaying PSP kernel to be given by $K(t) = V_0(\exp[-(t)/\tau] - \exp[-(t)/\tau_s])$, where $\tau$ is the synaptic current fall time constant and $\tau_s$ the synaptic current rise time constant. Our analysis is quite general and is applicable to other forms of the function $K$ as well. As mentioned earlier, the I&F output neuron elicits a spike when the voltage $V(t)$ crosses the threshold voltage $V_{thr}$. Let $n_{spk}$ denote the number of spikes fired by the output neuron for the presentation of a pattern. Then, the operation of the neuron is described as

$$\begin{aligned} &\text{If } V(t) > V_{thr}, \\ &V(t) \rightarrow 0 \\ &n_{spk}(t) = n_{spk}(t-1) + 1(n_{spk}(0) = 0) \end{aligned} \tag{2}$$

The final output of the network, $y$, is a logical variable having a value of 1 if the pattern is recognized. We define this operation by

$$\begin{aligned} y &= 1 \quad \text{if } n_{spk,final} > 0 \\ &= 0 \quad \text{otherwise} \end{aligned} \tag{3}$$

where $n_{spk,final}$ is the final value of $n_{spk}$ after the presentation of the pattern is completed. In other words, we declare the pattern recognized if the neuron fires one or more spikes in the entire duration.

### 2.2. Input pattern space

We mentioned earlier that the input spike pattern to the network is $\mathbf{x} = (x_1, x_2, \ldots, x_N)$ where $x_i \in [1\ T]$, $i = 1, 2, \ldots, N$. For any real world inputs, there is a finite precision $\Delta t$ at which an input $x_i$ can change.

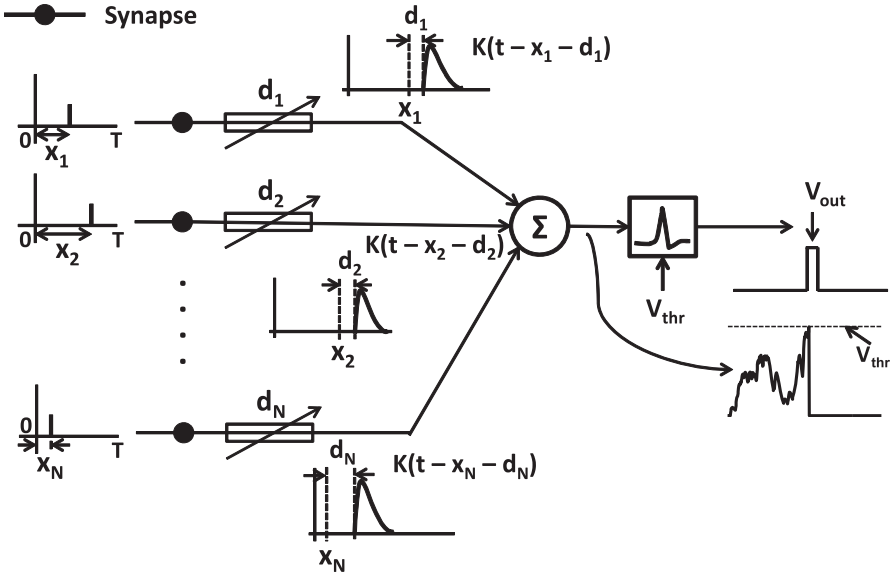


**Fig. 1.** Delay-based learning model where $N$ synaptic afferents receive incoming spikes fired at time $x_i$ and create EPSP waveforms delayed by $d_i$, $i = 1, 2, \ldots, N$. Spike delays $\mathbf{d} = (d_1, d_2, d_3, \ldots, d_N)$ are modified such that membrane potential $V(t)$ crosses the $V_{thr}$.