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Area-efficient robust Madaline based on continuous valued number system

Babak Zamanlooy*, Mitra Mirhassani

Department of Electrical and Computer Engineering, University of Windsor, Windsor, ON, Canada

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ABSTRACT

Achieving a low Noise-to-Signal Ratio (NSR) is one of the major concerns when implementing hardware-based neural networks. Continuous Valued Number System (CVNS) features have been exploited to improve the NSR. The efficiency of the network model in terms of area, power consumption, and NSR is measured using the product of the total number of neurons in the network multiplied by the network NSR, which indicates the number of neurons required for a specific NSR. The network proposed in this paper stores the weights in digital registers while the processing is done in the analog domain using CVNS arithmetic. The mathematical analysis and comparison between the proposed network and the previous structures prove that the proposed architecture improves upon in terms of both the NSR and the product of neuron multiplied by NSR.

1. Introduction

Since the advent of artificial neural networks, software and hardware implementation methods have been used for their realization. The hardware implementation methods have been exploited in applications that require real-time and energy-efficient processing [1–5].

Neural network hardware implementation methods may be classified as analog, digital or mixed-signal. In the analog implementation, both weight storage and processing are in the analog domain. When implemented by analog circuits, neural networks typically maintain a higher energy efficiency, a lower number of interconnections, and require less area, in comparison with its equivalent digital implementation. However, the capacitor-based weight storage methods require a refresh signal and are sensitive to process and power supply variations [6]. In the digital implementation of a neural network, both weight storage and processing are done in the digital domain. The third implementation method, mixed-signal, uses digital registers for weight storage and analog circuits for signal processing. This method exploits the ease of weight storage in digital registers while capitalizing on the advantages of analog domain such as compact addition and nonlinear neuron.

The basic theory behind the neural network can be essentially described as a series of weights, that when applied to distinct inputs, provide the appropriate corresponding output. Due to the limited word length available in hardware implementations of neural networks, inputs and weights are represented with finite precision; this degrades the output response. Therefore, the robustness to input and weight errors becomes a key issue in neural network architectures. To quantify this issue, the sensitivity of neural networks to input and weight imprecisions has been studied extensively [7–14].

The sensitivity analysis can be classified as one of the two approaches: the geometrical approach or the statistical approach. The geometrical method uses a hypersphere or a hyper-rectangle model to analyze the output sensitivity, while the statistical method determines the sensitivity by calculating the Noise-to-Signal Ratio (NSR). The NSR is defined as the ratio of the variance of output error to the variance of ideal output. Therefore, a network with a lower NSR is more tolerant to input and weight errors. In this paper, the statistical approach is utilized to study the effects of input and synaptic weight perturbations on the output.

Alternative number system can be exploited to design low NSR neural network architectures. The Continuous Valued Number System (CVNS) is a mixed-signal number system in which its analog digits share information. This feature enables multiple error correction in a digit set [15] and makes this number system a candidate for implementing analog/mixed-signal neural networks with a low NSR [16–18].

A CVNS neural network is presented in [16]. This structure is analog, in which the synaptic weights are stored in the CVNS format and processing is accomplished using CVNS arithmetic. To decrease the output error, the output of the Adaline is

* Corresponding author. Tel.: +1 519 992 0240.
E-mail addresses: zamanlo@uwindsor.ca (B. Zamanlooy), mitramir@uwindsor.ca (M. Mirhassani).

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Nomenclature

$\sigma^2_{\Delta w}/\sigma^2_w$	weight Noise to Signal Ratio
$\sigma^2_{\Delta x}/\sigma^2_x$	input Noise to Signal Ratio
$\sigma^2_{\Delta y}/\sigma^2_y$	output Noise to Signal Ratio
σ_w	weight standard deviation
σ_x	input standard deviation
B	radix of CVNS digits
$D+1$	number of CVNS digits
g	stochastic gain function
g'''	stochastic gain function of CVNS fully distributed Madaline
g''	stochastic gain function of CVNS distributed Madaline
g'	stochastic gain function of distributed Madaline
$L+1$	number of Madaline layers
N	number of Adaline inputs
N_{CDM}	number of neurons of the CVNS distributed Madaline
N_{CFDM}	number of neurons of the CVNS fully distributed Madaline
N_{CREM}	number of neurons of the CVNS-RE Madaline
N_{DM}	number of neurons of distributed Madaline
N_i	number of Adalines in layer i of Madaline
N_{LM}	number of neurons of lumped Madaline
N_{PM}	number of neurons of proposed Madaline
NSR_{CDM}	Noise to Signal Ratio of CVNS distributed Madaline
NSR_{CFDM}	Noise to Signal Ratio of CVNS fully distributed Madaline
NSR_{CREM}	Noise to Signal Ratio of CVNS-RE Madaline
NSR_{DM}	Noise to Signal Ratio of distributed Madaline
NSR_{LM}	Noise to Signal Ratio of lumped Madaline
NSR_{PA}	Noise to Signal Ratio of proposed Adaline
NSR_{PM}	Noise to Signal Ratio of proposed Madaline

generated based on the Reverse Evolution (RE) process [15]. This architecture is referred to as CVNS-RE in the rest of this paper.

Using the information redundancy present in the CVNS and the distributed neuron structure, two architectures named CVNS-DNN and CVNS-FDNN were developed in [17]. Similar to the CVNS-RE architecture, both of these structures store the weights in the CVNS format while the processing is carried out using CVNS arithmetic.

The previously developed CVNS neural network architectures [16–18] store synaptic weights in analog memories which require a refresh signal and are sensitive to process and power supply variations. Moreover, the NSR improvement of the previous architectures is achieved at the cost of extra neurons, which results in area overhead and increased power consumption. Although NSR is generally a suitable measure to show the effect of input and weight errors on the network output, the efficiency of different architectures cannot be measured by this quantity alone. A better indicator of the efficiency of a network model is the product of the total number of neurons in the network multiplied by the network NSR, this provides a better estimate in terms of area and power consumption for a specific NSR level.

To investigate the efficiency of various Madaline architectures based on the previous CVNS Adalines, mathematical analysis of NSR and neuron × NSR of these architectures is required. It is worth noting that only the NSR of CVNS Adalines has been considered previously. The mathematical analysis performed in this paper allows the efficiency evaluation of different neural network architectures.

In this paper, a new mixed-signal Adaline is proposed. The proposed architecture stores the weights in digital registers while the arithmetic is based on the CVNS number system. Using digital registers to store weights eliminates the need for a refresh signal and provides a process and power supply variation tolerant storage mechanism, eliminating the problems caused by the analog weight storage methods used in the previous CVNS structures [16–18].

In the previously developed CVNS networks, the total number of analog memories required for each Adaline is proportional to the number of CVNS digits representing the synaptic weights. However, the total number of registers in the proposed CVNS Adaline is independent of the number of CVNS digits. This in turn results in reduced weight storage elements which lead to lower area overhead and lower power consumption. Furthermore, the RE process is used to decrease the error in the CVNS digits, which improves the NSR.

Using the proposed Adaline, a Madaline named CVNS-distributed is proposed. The CVNS-distributed Madaline uses the proposed CVNS Adaline at its output layer. The NSR and the neuron × NSR of the proposed Madaline is formulated and compared with conventional lumped and distributed as well as previous CVNS structures. This analysis proves that the proposed architecture is more immune to input and weight errors while simultaneously requiring a lower number of neurons for a specific NSR, resulting in an architecture with a lower area overhead and lower power consumption. In this research, a three-layer Madaline is implemented in TSMC CMOS 0.18 μm. The implementation results confirm the advancement of the proposed Madaline in terms of NSR and the area consumption required for a specific NSR.

The rest of this paper is organized as follows. In the next section, CVNS is briefly introduced. The NSR and the stochastic model proposed by Piche [10] is briefly discussed in Section 3. Moreover, the NSR of previous Adalines is summarized in this section. The mathematical derivation of the total number of neurons and NSR of a Madaline, based on the previous structures, is provided in Section 4, where the related equations are developed. The proposed Adaline and Madaline structure is explained in Section 5. Comparisons with existing structures are carried out in Section 6. The VLSI implementation of a three-layer Madaline and comparisons with previous structures are conducted in Section 7. Finally, conclusions are drawn in Section 8.

2. Continuous Valued Number System (CVNS)

The absolute value of a real number x using fixed-point number representation with a radix of B can be shown as follows:

$$x = \sum_{i=-N_f}^{N_i-1} x_i \times B^i \tag{1}$$

where N_i and N_f are the number of integer and fractional digits, respectively while x_i is the digit.

CVNS is a number system with continuous valued digits. CVNS analog digits representing the real number x can be generated as follows [15]:

$$((x))_i = (x \times B^{-i}) \bmod B \tag{2}$$

where $((x))_i$ is the CVNS digit and $-N_f \le i \le N_i - 1$. An ensemble of CVNS digits $((x))_= \{((x))_{N_i-1}, \ldots, ((x))_0, ((x))_{-1}, \ldots, ((x))_{-N_f}\}$ represents the input x in CVNS format.

Example: Finding the CVNS digit set of $x=81.92$ with a radix of 10.