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Letters

Synaptic memcapacitor bridge synapses

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ABSTRACT

In this article, a memcapacitor bridge circuit consisting of four identical memcapacitors is proposed. With this circuit, we can perform positive, negative and zero synaptic weightings. Weight programming is performed in a memcapacitor bridge circuit, while weight-multiplication processing is performed in a memcapacitor bridge synapse circuit. The current pulse is used in weight programming while the voltage pulse is used in weight-multiplication processing. Simulations are done with a nonlinear drift memcapacitor model.

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1. Introduction

Leon Chua mathematically predicted the fourth fundamental circuit element in 1971, which is characterised by a relationship between charge and flux linkage. [1] In the article 'Memristive devices and systems' published in 1976, Leon Chua and Sung Mo Kang generalised the theory of memristors and memristive systems. [2] Chua also defined other hypothetical 'mem-elements' at the 'Memristor and Memristive Systems Symposium' in December 2008 [3]; the memcapacitor and the meminductor in particular, which compared with the memristor, have the advantage of lossless data reading and storing. Memcapacitive and meminductive systems are defined in detail in Ref. [4]. The methodology of a memcapacitor is given in Ref. [5]. A memristor-to-memcapacitor mutator was designed by means of off-the-shelf circuits in Ref. [6]. A methodology for Simulation Program with Integrated Circuit Emphasis (SPICE) modelling of a memcapacitor is described in Ref. [7]. Frequency-domain models of a memristor, memcapacitor and meminductor and steady-state analysis by means of the harmonic-balance method are described in Ref. [8].

There are more than 100 billion neurons in the human brain and each neuron has more than 20,000 synapses. [9] Efficient circuit implementation of synapses is very important for building a brain-like machine. The cellular neural network (CNN)[10] is known as one of the successful approaches. Recently, a pulse-based programmable memristor circuit for implementing synaptic weights for artificial neural networks was proposed in Ref. [11]. A memristor-based synaptic circuit consisting of four identical memristors in a bridge circuit capable of executing both positive and negative weightings, via pulses, is described in Ref. [12].

Compared with the memristor, the memcapacitor loses data to a lesser extent in data reading and storing. Therefore, in this article, we propose a memcapacitor-based synapse consisting of a four-memcapacitor bridge circuit and three transistors. Strong (large and wide) pulses are used for programming the synaptic weights, while weak (small or narrow) pulses having negligible effects on the memcapacitor operating point are used as processing input signals.

In Section 2, we review the principle and the mathematical model of the memcapacitor. Section 3 introduces a memcapacitor bridge synaptic circuit. The weight programming is executed in Section 4. The simulation results and conclusion are given in Sections 5 and 6, respectively.

2. Memcapacitor

According to Ref. [7], the general equation of the capacitor with varying memcapacitance C_M is

$$C_M(t)v(t) = C_M(0)v(0) + \int_0^t i(\xi)d\xi \tag{1}$$

where $v(0)$ is the initial voltage at time 0; using the inverse memcapacitance,, the equation can be rewritten as follows:

$$v(t) = D_M(t)\left[C_M(0)v(0) + \int_0^t i(\xi)d\xi\right] \tag{2}$$

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This equation shows a sketch of the memcapacitor, the memcapacitance of which is adjustable by the width of its dielectric. [7] The width L can vary within the limits from $L_{\min}$ to $L_{\max}$ to, with the corresponding limit memcapacitances and inverse memcapacitances $C_{M,\max}$,$C_{M,\min}$, and $D_{M,\min}$, $D_{M,\max}$. Let us define the state variable x of such a memcapacitive system as follows:

$$x=\frac{L-L_{\min}}{L_{\max}-L_{\min}}\in(0,1) \tag{3}$$

Then, the inverse memcapacitance will depend on the state variable according to the formula

$$D_M(t)=D_{M,\min}+(D_{M,\max}-D_{M,\min})x(t) \tag{4}$$

According to Ref. [7], consider the state equation of the charge-controlled memcapacitor in the form

$$\dot{x}(t)=kq(t)\text{window}(x) \tag{5}$$

where the ratio of the change of the dielectric width is directly proportional to the charge being conveyed and to the mobility factor k. The nonlinear function window(x) guarantees that this ratio will tend to zero when the dielectric width approaches its physical limits $L_{\min}$ and $L_{\max}$. In this article, we use the Joglekar window function [13]

$$\text{window}(x)=1-(2x-1)^{2p} \tag{6}$$

where p is a positive integer.

3. Memcapacitor Bridge Synaptic Circuit

The memcapacitor bridge circuit consists of four identical memcapacitors and the polarity of each memcapacitor is indicated in Fig. 1. When a positive strong pulse is applied as input, the inverse memcapacitance of D_{M_1} and D_{M_4} (whose polarities are reverse biased) will decrease. However, the inverse memcapacitance of D_{M_2} and D_{M_3} (whose polarities are forward biased) will increase. Therefore, the voltage V_A at node A (with respect to ground) becomes larger than the voltage V_B at node B. In this case, the circuit produces a positive output voltage V_{out} and represents a positive synaptic weight.

However, when a negative strong pulse is applied, the inverse memcapacitances are varied in the opposite direction and the voltage at node B becomes larger than that at node A. In this case, the circuit produces a negative output voltage V_{out} and represents a negative synaptic weight.

The memcapacitor bridge synaptic circuit is shown in Fig. 2. It consists of the memcapacitor bridge circuit and three additional transistors. The differential amplifier with three transistors functions as a current source, which can be used to convert voltage to current.

Suppose an input pulse V_{in} is applied to the memcapacitor bridge circuit shown in Fig. 1 at time t. At this time, the memcapacitor bridge acts like a linear capacitor network. We can obtain four equations via

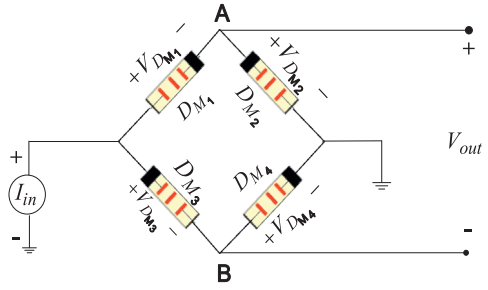

Fig. 1. Memcapacitor bridge circuit. The synaptic weight is programming with the input current I_{in} in this circuit.

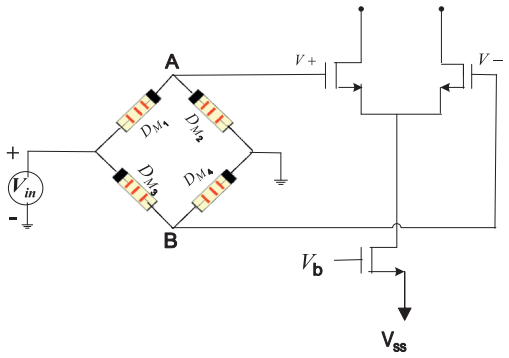

Fig. 2. Memcapacitor bridge synaptic circuit. The weighting (multiplication) of the input voltage V_{in} is performed in this circuit.

the 'capacitor-series formula' and 'voltage-divider formula' as follows:

$$V_{D_{M_1}}=\frac{D_{M_1}}{D_{M_1}+D_{M_2}}V_{in} \tag{7a}$$

$$V_{D_{M_2}}=\frac{D_{M_2}}{D_{M_1}+D_{M_2}}V_{in} \tag{7b}$$

$$V_{D_{M_3}}=\frac{D_{M_3}}{D_{M_3}+D_{M_4}}V_{in} \tag{7c}$$

$$V_{D_{M_4}}=\frac{D_{M_4}}{D_{M_3}+D_{M_4}}V_{in} \tag{7d}$$

whereD_{M_1}, D_{M_2}, D_{M_3} and D_{M_4} denote the corresponding inverse memcapacitances of the memcapacitors at time t, shown in Fig. 1.

The output voltage V_{out} of the memcapacitor bridge circuit is equal to the voltage difference between terminal A and terminal B, namely

$$V_{out}=V_{AB}=V_{D_{M_2}}-V_{D_{M_4}}=\left[\frac{D_{M_2}}{D_{M_1}+D_{M_2}}-\frac{D_{M_4}}{D_{M_3}+D_{M_4}}\right]V_{in} \tag{8}$$

Eq. (8) can be rewritten as a relationship

$$V_{out}=\psi\times V_{in} \tag{9}$$

between the synaptic weight ψ and synaptic input signal V_{in}, where

$$\psi=\frac{D_{M_2}}{D_{M_1}+D_{M_2}}-\frac{D_{M_4}}{D_{M_3}+D_{M_4}} \tag{10}$$

Eqs. (9) and (10) define the synaptic-weighting operation in the memcapacitor bridge circuit. Since the bridge acts like a linear capacitor network during short time intervals, the weighting operation is almost linear. The detailed analysis of the linearity in the synaptic-weight programming will be carried out in the next section.

According to Ref. [12], we also can design a memcapacitor bridge neuron circuit which is analogous to the memristor bridge neuron. In this article, we only realise the simulation of a synaptic circuit. Therefore, we have not provided the circuit design of the neuron. If possible, we will investigate it in the future.

4. Weight Programming in Memcapacitor Bridge Circuit

The synaptic-weight processing was performed with very small or narrow pulses so that its effect on the change in the memcapacitor was negligible. By contrast, the pulses for synaptic-weight programming must be strong enough to change the charge operating point of the memcapacitor.

If the synaptic weight ψ is larger than 0, namely

$$\psi=\frac{D_{M_2}}{D_{M_1}+D_{M_2}}-\frac{D_{M_4}}{D_{M_3}+D_{M_4}}>0 \tag{11}$$

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