# Separator-based graph embedding into multidimensional grids with small edge-congestion 

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#### Abstract

We study the problem of embedding a guest graph with minimum edge-congestion into a multidimensional grid with the same size as that of the guest graph. Based on a well-known notion of graph separators, we show that an embedding with a smaller edge-congestion can be obtained if the guest graph has a smaller separator, and if the host grid has a higher but constant dimension. Specifically, we prove that any graph with $N$ nodes, maximum node degree $\Delta$, and with a node-separator of size $s$, where $s$ is a function such that $s(n)=O\left(n^{\alpha}\right)$ with $0 \leq \alpha<1$, can be embedded into a grid of a fixed dimension $d \geq 2$ with at least $N$ nodes, with an edge-congestion of $O(\Delta)$ if $d>1 /(1-\alpha), O(\Delta \log N)$ if $d=1 /(1-\alpha)$, and $O\left(\Delta N^{\alpha-1+\frac{1}{d}}\right)$ if $d<1 /(1-\alpha)$. This edge-congestion achieves constant ratio approximation if $d>1 /(1-\alpha)$, and matches an existential lower bound within a constant factor if $d \leq 1 /(1-\alpha)$. Our result implies that if the guest graph has an excluded minor of a fixed size, such as a planar graph, then we can obtain an edge-congestion of $O(\Delta \log N)$ for $d=2$ and $O(\Delta)$ for any fixed $d \geq 3$. Moreover, if the guest graph has a fixed treewidth, such as a tree, an outerplanar graph, and a series-parallel graph, then we can obtain an edge-congestion of $O(\Delta)$ for any fixed $d \geq 2$. To design our embedding algorithm, we introduce edge-separators bounding extension, such that in partitioning a graph into isolated nodes using edge-separators recursively, the number of outgoing edges from a subgraph to be partitioned in a recursive step is bounded. We present an algorithm to construct an edge-separator with extension of $O\left(\Delta n^{\alpha}\right)$ from a node-separator of size $O\left(n^{\alpha}\right)$.


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## 1. Introduction

A graph embedding of a guest graph into a host graph is to map (typically one-to-one) nodes and edges of the guest graph onto nodes and paths of the host graph, respectively, so that an edge of the guest graph is mapped onto a path connecting the images of end-nodes of the edge. The graph embedding problem is to embed a guest graph into a host graph with certain constraints and/or optimization criteria. This problem has applications such as efficient VLSI layout and parallel computation. I.e., the problem of efficiently laying out VLSI can be formulated as the graph embedding problem with modeling a design rule on wafers and a circuit to be laid out as host and guest graphs, respectively. Also, the problem of efficiently implementing a parallel algorithm on a message passing parallel computer system consisting of processing elements connected by an interconnection network can be formulated as the graph embedding problem with modeling the interconnection network and interprocess communication in the parallel algorithm as host and guest graphs, respectively. See for a survey, e.g., [26]. The major criteria to measure the efficiency of an embedding are dilation,

[^0]Table 1
Previous results of graph embeddings minimizing edge-congestion.

| Guest graph <br> $N$ : \# nodes, $\Delta$ : max degree <br> $s$ : separator size | Host grid |  | Congestion | Dilation |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | \# nodes | dimension |  |  |  |
| Connected planar graph | $N$ | 2 | NP-hard for 1 | any | [11] |
| Connected graph | $2^{\left\lceil\log _{2} N\right\rceil}$ | $\left\lceil\log _{2} N\right\rceil$ | NP-hard for 1 | any | [16] |
| Complete binary tree | $N+1$ | 2 | 2 | $O(\sqrt{N})$ | [32] |
| Complete binary tree | $N+1$ | 4 | 1 | $O\left(N^{1 / 4}\right)$ | [19] |
| Complete binary tree | $N+O(\sqrt{N})$ | 2 | 1 | $O(\sqrt{N})$ | [13] |
| Complete $k$-ary tree ( $k \geq 3$ ) | $N+O(N / \sqrt{k})$ | 2 | $\lceil k / 2\rceil+1$ | $O(\sqrt{N})$ | [29] |
| Binary tree | $2^{\left\lceil\log _{2} N\right\rceil}$ | $\left\lceil\log _{2} N\right\rceil$ | 5 | $\left\lceil\log _{2} N\right\rceil$ | [24] |
| 2 -D $h \times w$-grid ( $h \leq w$ ) | $h^{\prime} w^{\prime} \geq N^{\text {a }}$ | 2 | $\left\lceil h / h^{\prime}\right\rceil+1$ | $\left\lceil h / h^{\prime}\right\rceil+1$ | [27] |
| 2-D $h \times w$-grid ( $h \leq w$ ) | $h^{\prime} w^{\prime} \geq N^{\mathrm{b}}$ | 2 | 5 | 5 | [27] |
| 2-D $h \times w$-grid ( $h \leq w$ ) | $h^{\prime} w^{\prime} \geq N^{\mathrm{b}}$ | 2 | 4 | $\geq 4 h-3$ | [27] |
| 2-D grid | $2^{\left\lceil\log _{2} N\right\rceil}$ | $\left\lceil\log _{2} N\right\rceil$ | 2 | 3 | [28] |
| $\Delta \leq 4, s=O\left(n^{\alpha}\right), \alpha<1 / 2$ | $\mathrm{O}(\mathrm{N})$ | 2 | 1 | $O(\sqrt{N} / \log N)$ | [7] |
| $\Delta \leq 4, s=O(\sqrt{n})$ | $O\left(N \log ^{2} N\right)$ | 2 | 1 | $O\left(\frac{\sqrt{N} \log N}{\log \log N}\right)$ | [7] |
| $\Delta \leq 4, s=O\left(n^{\alpha}\right), \alpha>1 / 2$ | $O\left(N^{2 \alpha}\right)$ | 2 | 1 | $O\left(N^{\alpha}\right)$ | [7] |
| tree width $t$ | $2^{\left\lceil\log _{2} N\right\rceil}$ | $\left\lceil\log _{2} N\right\rceil$ | $O\left(\Delta^{4} t^{3}\right)$ | $O(\log (\Delta t))$ | [14] |
| $s=\log ^{O(1)} N$ | $2^{\left\lceil\log _{2} N\right\rceil}$ | $\left\lceil\log _{2} N\right\rceil$ | $\Delta^{O(1)}$ | $O(\log \Delta)$ | [15] |
| $\Delta=O(1)$ | $N$ | $d=O(1)$ | $O\left(N^{1 / d} \log N\right)$ | $O\left(N^{1 / d} \log N\right)$ | [21] |
| $\Delta \leq 2\left\lceil\log _{2} N\right\rceil$ | $2^{2\left\lceil\log _{2} N\right\rceil}$ | $2\left\lceil\log _{2} N\right\rceil$ | 1 | $2\left\lceil\log _{2} N\right\rceil$ | [24] |

[^1]node-congestion, and edge-congestion, load, and expansion, whose formal definitions are given in Section 2 . In this paper, we consider the problem of embedding a guest graph with the unit load and minimum edge-congestion into a $d$-dimensional grid with $d \geq 2$ and the same size as that of the guest graph (i.e., with unit expansion). Embeddings into grids with the minimum edge-congestion are important for both VLSI layout and parallel computation. Actually, design rules on wafers in VLSI are usually modeled as 2-dimensional grids, and the minimum edge-congestion provides a lower bound on the number of layers needed to lay out a given circuit. As for parallel computation, multidimensional grid networks, including hypercubes, are popular for interconnection networks. On interconnection networks adopting circuit switching or wormhole routing, in particular, embeddings with the edge-congestion of 1 are essential to minimize the communication latency $[16,19,29]$. In addition, the setting that host and guest graphs have the same number of nodes is important for parallel computation because the processing elements are expensive resource and idling some of them is wasteful.

## Previous results

Graph embedding into grids with small edge-congestion has extensively been studied. Table 1 summarizes previous results of graph embeddings minimizing edge-congestion (and other criteria as well in some results) for various combinations of guest graphs and host grids.

VLSI layout has been studied through formulating the layout as the graph embedding into a 2-dimensional grid with objective of minimizing the grid under constrained congestion-1 routing [30]. Leiserson [22] and Valiant [31] independently proposed such embeddings based on graph separators. In particular, it was proved in [22] that any $N$-node graph with maximum node degree at most 4 and an edge-separator of size $s$, where $s$ is a function with $s(n)=O\left(n^{\alpha}\right)$, can be laid out in an area of $O(N)$ if $\alpha<1 / 2, O\left(N \log ^{2} N\right)$ if $\alpha=1 / 2$, and $O\left(N^{2 \alpha}\right)$ if $\alpha>1 / 2$. A separator of a graph $G$ is a set $S$ of either nodes or edges whose removal partitions the node set $V(G)$ of $G$ into two subsets of roughly the same size with no edge between the subsets. The graph $G$ is said to have a (recursive) separator of size $s(n)$ if $|S| \leq s(|V(G)|)$ and the subgraphs partitioned by $S$ recursively have separators of size $s(n)$. Separators are important tools to design divide-and-conquer algorithms and have been extensively studied. Bhatt and Leighton [7] achieved a better layout with several nice properties including reduced dilation as well as the same or better area as that of [22] by introducing a special type of edge-separators called bifurcators. An approximation algorithm for VLSI layout was proposed in [9]. Separator-based graph embeddings on hypercubes were presented in $[6,25,15]$. In particular, Heun and Mayr [15] proved that any $N$-node graph with maximum node degree $\Delta$ and an extended edge-bisector of polylogarithmic size can be embedded into a $\left\lceil\log _{2} N\right\rceil$-dimensional cube with a dilation of $O(\log \Delta)$ and an edge-congestion of $\Delta^{O(1)}$.

A quite general embedding based on the multicommodity flow was presented by Leighton and Rao [21], who proved that any $N$-node bounded degree graph $G$ can be embedded into an $N$-node bounded degree graph $H$ with both dilation and edge-congestion of $O((\log N) / \alpha)$, where $\alpha$ is the flux of $H$, i.e., $\min _{U \subset V(H)} \frac{|\{(u, v) \in E(H) \mid u \in U, v \in V(H) \backslash U\}|}{\min \{|U|,|V(H) \backslash U|\}}$. This implies that $G$ can be embedded into an $N$-node $d$-dimensional grid with both dilation and edge-congestion of $O\left(N^{1 / d} \log N\right)$ for any fixed $d$.

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[^1]:    ${ }^{\text {a }} h^{\prime} \times w^{\prime}$-grid with $h^{\prime}<h \leq w<w^{\prime}$.
    ${ }^{\text {b }} h^{\prime} \times w^{\prime}$-grid with $h<h^{\prime} \leq w^{\prime}<w$.

