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Parameter variation sensing and estimation in nanoscale fabrics

Jianfeng Zhang *, Mostafizur Rahman, Pritish Narayanan, Santosh Khasanvis, C. Andras Moritz

Department of Electrical and Computer Engineering, University of Massachusetts Amherst, Amherst, MA 01003, USA

HIGHLIGHTS

- A novel variation sensor for nanoscale computing fabrics is proposed.
- Detailed on-chip random parameter variation sensing methodology is presented.
- An evaluation framework based on HSPICE Monte Carlo simulations is presented.
- Sensor accuracy was found to be 8% on average and 12.7% in the worst case.

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ABSTRACT

Parameter variations introduced by manufacturing imprecision are becoming more influential on circuit performance. This is especially the case in emerging nanoscale computing fabrics due to unconventional manufacturing steps and aggressive scaling. On-chip variation sensors are gaining in importance since post-fabrication compensation techniques can be employed. In estimation with on-chip variation sensors, however, random variations are masked because of well-known averaging effects during measurements. We propose a new on-chip sensor for nanoscale computing fabrics to estimate random variations in physical parameters. We show detailed estimation methodology and validate it with Monte Carlo simulations. The results show the sensor estimation error to be 8% on average and 12.7% in the worst case. In comparison to the well-known ring-oscillator based approach developed for CMOS, the estimation accuracy is 1.6× better and requires 40× less devices in on-chip sensors.

1. Introduction

Emerging nanoscale computing systems have been proposed as an alternative to scaled CMOS with potential performance and density benefits. These nanoscale computing systems are based on novel nanostructures, such as nanowires [22,23], carbon nanotubes [4], graphene [5,6], electromagnetic devices [16–18], etc. Their manufacturing approaches incorporate unconventional (e.g., self-assembly, nano-imprint) and conventional (e.g., deposition, etching, and lithography) process steps. As their feature sizes shrink into deep nanoscale, the manufacturing process may cause a significant level of variations in physical parameters. For example, during dopant implantation, there exists some randomness in the distribution of dopants, which can result in the fluctuation of the total number of dopants in a specified region. These variations could potentially lead to performance deterioration such as timing errors and consequently yield loss.

Parameter variations are traditionally addressed pre-fabrication by circuit design, often targeting worst-case variation scenarios. However, this pre-fabrication approach is pessimistic and performance benefits can be lost especially for nanoscale fabrics where the extent of variability can be high. Alternatively, if parameter variations could be estimated post-fabrication, some compensation techniques, such as redundant intermediate bitslices [13] and dynamic fine-grain body biasing [20], could be used to adjust circuit timing and reduce leakage power during run-time, leading to area and performance benefits.

Conventional variation estimation methods [21,7] assume that large circuits are not affected by random variations because of an averaging effect; i.e., the influence of random variations is assumed to be nullified if the number of transistors in the critical path is large [1]. However, at nanoscale the impact of random variations cannot be neglected, since the influence is non-linear on circuit performance. For example, in [12] it was shown that there exists a non-linear relationship between the on-current of devices and random variations in certain parameters (e.g., channel doping, source–drain doping and underlap). The system level performance was shown to degrade considerably as a result of random variations, with 67% of simulated chips operating at less than their

* Corresponding author.
E-mail addresses: zljmfy@gmail.com, zljmfy@126.com (J. Zhang).

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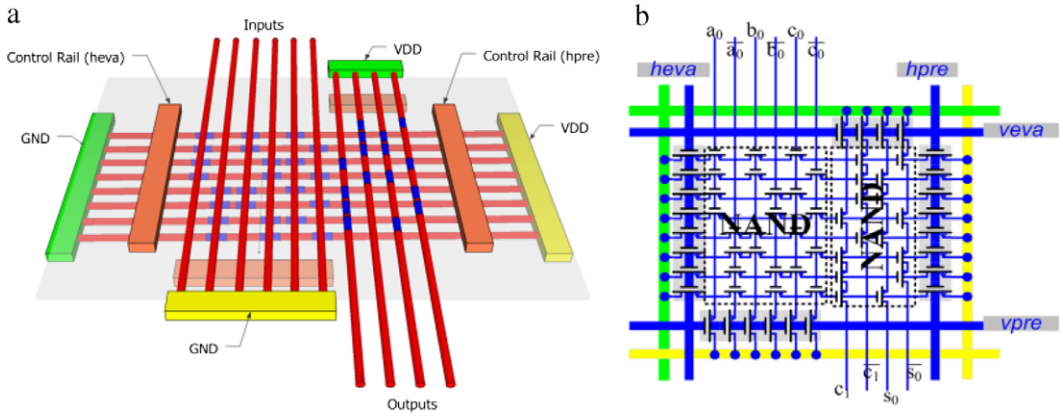

Fig. 1. Nanoscale application specific integrated circuits with regular semiconductor nanowire grids, xnwFET devices and peripheral microscale control: (a) 3-D fabric view, (b) circuit schematic.

nominal frequency [12]. Therefore, we believe that in order to estimate parameter variations accurately, random variations should be explicitly taken into consideration.

In this paper we propose a novel on-chip sensor design for quantifying the statistical distribution and impact of random variations in physical parameters for the Nanoscale Application Specific Integrated Circuits (NASICs) fabric [9–11,24,8]. The proposed sensor can estimate the statistical distribution of random variations in physical parameters in a chip from its own variations. This is also possible because NASICs rely on a uniform array-based structure with identical devices and no arbitrary sizing or doping; consequently, this implies that sensor circuits designed with the same devices and logic styles can represent the fabric as a whole. This sensor design and methodology is also directly applicable to the Nanoscale 3-D Application Specific Integrated Circuits (N^3ASICs) [14,15], and the methodology can be extended to other regular nanoscale fabrics in general.

We first explain the principles of sensor design, and describe the methodology for variability sensing. In our sensor, signal fall and rise times are used to extract the statistical distribution of random variations in different physical parameters. These fall and rise times can be easily and accurately measured by some existing approaches as shown in [2]. Further, we present a methodology for evaluating and validating this sensor design using Monte Carlo circuit simulations. The simulation results obtained from 150 variation sensors show that the relative error between the injected and estimated standard deviation of physical parameters is 12.7% in the worst-case and 8% on average scenarios. Compared with the ring-oscillator (RO) based sensor design in CMOS technology shown in [19], the worst-case estimation error is improved by 1.6×, and the total number of devices required in on-chip sensors is reduced by 40×.

The rest of this paper is organized as follows: Section 2 briefly presents the NASIC fabric with emphasis on physical parameter variation; Section 3 illustrates the new sensor design and discusses the theoretical framework for estimating the distribution of random variations in physical parameters; Section 4 describes the Monte Carlo simulation methodology for evaluating the sensor design; simulated results for the sensor accuracy are shown in Section 5; and Section 6 concludes the paper.

2. NASICs fabric overview

Nanoscale Application Specific Integrated Circuits (NASICs) is a nanoscale computational fabric that relies on 2-D grids of semiconductor nanowires with crossed nanowire field-effect transistors (xnwFETs) at certain crosspoints (Fig. 1). In this fabric, in order to ease manufacturing requirements, a regular grid layout is used where all transistors on the crosspoints are identical with no arbitrary doping or sizing requirements. This semiconductor nanowire grid includes some peripheral microwires to carry *VDD*, *GND* and control signals. Dynamic circuit styles without the requirement of complementary devices or arbitrary placement/sizing are used for logic implementation. Several extensions exist to NASICs and there are other circuit styles also proposed but the approach for variability estimation applies across all of them.

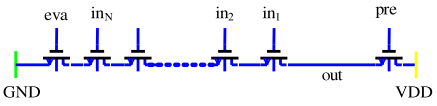

Fig. 2. *N-input* NASIC dynamic NAND gate.

The dynamic circuit style and xnwFET structure are shown in Figs. 2 and 3. Fig. 2 shows an *N-input* dynamic NAND gate with xnwFETs as active devices. The *pre* and *eva* signals in this NAND gate are used to precharge and discharge the output (*out*), respectively, depending on inputs (in_1, in_2, . . . , in_N). Multiple stages of logic can be achieved by cascading multiple such dynamic NAND gates. The proposed sensor follows the same dynamic circuit style.

The assumed xnwFET device operating principle in this paper is similar to that of inversion mode devices; the current through the channel nanowire is modulated by the potential applied on the orthogonal gate. Sources of random variations in this xnwFET structure include channel doping (*CD*), source–drain doping (*SDD*) and underlap (*U*). In this paper, random variations in *CD*, *SDD* and *U* are considered; systematic variation (e.g., channel/gate diameter, gate/bottom oxide thickness) estimation was shown in our previous paper [25].

3. On-chip variation sensor design

A key motivation for a novel on-chip sensor design is that a conventional RO-based sensor design may be unsuitable for random-variation estimation in these emerging fabrics. This is mainly because: (i) the RO frequency averages the parameters of transistors in all stages and cannot thus accurately represent the characterization of random variations on individual devices; and (ii) RO-based sensors occupy a large fraction of chip area since the number of RO stages required is typically more than 100 for each sensor.

In this section, we discuss a new on-chip sensor design in the context of the NASIC fabric. The sensor can be used to estimate the statistical distribution of random variation in physical parameters based on the measured fall time (1-*to*-0 transitions) and rise time (0-*to*-1 transitions) from the sensor circuit.