



Short communication

A FPGA real-time model of single and multiple visual cortex neurons

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ABSTRACT

Using a biologically realistic model of a single neuron can be very beneficial for visual physiologists to test their electrophysiology setups, train students in the laboratory, or conduct classroom-teaching demonstrations. Here we present a Field Programmable Gate Array (FPGA)-based spiking model of visual cortex neurons, which has the ability to simulate three independent neurons and output analog spike waveform signals in four channels. To realistically simulate multi-electrode (tetrode) recordings, the independently generated spikes of each simulated neuron has a distinct waveform, and each channel outputs a differentially weighted sum of these waveforms. The model can be easily constructed from a small number of inexpensive commercially available parts, and is straightforward to operate. In response to sinusoidal grating stimuli, the neurons exhibit biologically realistic simple-cell-like response properties, including highly modulated Poisson spike trains, orientation selectivity, spatial/temporal frequency selectivity, and space-time receptive fields. Users can customize their model neurons by downloading modifications to the FPGA with varying parameter values, particularly desired features, or qualitatively different models of their own design. The source code and documentation are provided to enable users to modify or extend the model's functionality according to their individual needs.

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1. Introduction

A realistically behaving physical model of a primary visual cortex neuron can be useful for classroom-teaching and for training students in the research laboratory. Such a model would also be beneficial to visual physiologists by helping to ensure smooth operation of experiments through proper evaluation of electrophysiological recording setups (including data acquisition, data analysis, and stimulus presentation). Incorporating the ability to simulate multi-electrode recordings of multiple neurons would further enhance the power of such a model.

Earlier neuron models that met some of these objectives were based on hardware, software, or custom integrated circuits. Most hardware-implemented models require numerous resistors, capacitors, and transistors (French and Stein, 1970) or integrated circuit chips (Rebrik and Miller, 2004; Schweitzertong, 1983) on a breadboard or homemade printed circuit board, making the device difficult to build, awkward to modify, and potentially unreliable. Software models such as the Visual Neuron Simulator (Peterson and Ohzawa, 1999; Saito et al., 2008) have been well-suited to classroom demonstrations, but did not provide electrical signals

for testing electrophysiological recording systems. Even with the addition of hardware extensions, a software simulator might still have difficulty providing real-time responses from complex models or multi-unit simulations.

The “Physiologist’s Friend” (Delbruck and Liu, 2004) is a technologically impressive model neuron for visual neurophysiologists, based on a custom-designed analog VLSI (Very-Large-Scale Integration) circuit. This model was designed as a biologically realistic simulation of early retinal processing, including automatic gain control to provide robustness for background lighting conditions. The output simulates spiking responses of retinal ganglion cells or visual cortex neurons to visual stimuli presented in its receptive field. However the use of a VLSI chip makes it impossible for the user to modify the model, and availability is limited due to the complex design process and special facilities required for fabrication.

To overcome the limitations of the models mentioned above and to incorporate new model features, for example multi-unit responses and multi-channel signal outputs, a higher performance simulator would be useful. It should be easily constructed from a small number of inexpensive commercially available parts, and be user-extensible without elaborate or specialized circuit fabrication.

A Field Programmable Gate Array (FPGA) addresses these issues by offering a high performance, configurable platform for building hardware model neurons. A FPGA is a programmable device consisting of a reconfigurable array of logic elements and a customizable hierarchy of interconnects that allows the logic elements to be tailored to a particular application and to be modified repeat-

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edly, somewhat like a one-chip programmable breadboard. The FPGA is reconfigured using hardware description languages (HDLs), which are not specific to a particular FPGA chip – thus code developed for one chip can be easily moved to another with only minor adjustments. Because of broad commercial development and support for FPGA technologies as well as the transportability of HDL code, this approach to neural modeling should be considerably cheaper and less vulnerable to obsolescence of hardware or operating systems. Finally, the inherent parallelism of the logic elements on a FPGA allows for a fully parallel approach to designing a multi-neuron model, providing the potential to run simulations in real-time and much faster than conventional software models. Previous FPGA neural models (Guerrero-Rivera et al., 2006; Pearson et al., 2007; Weinstein et al., 2007) demonstrated the power of this approach, but did not include visual inputs, simulations of visual cortex receptive fields, or outputs suitable for testing electrophysiology setups.

Here we present a FPGA-based model of one or more visual cortex neurons. The model is not intended to be biologically realistic in its internal computations, but only to simulate an “LNP” (Linear-Nonlinear-Poisson) model (Schwartz et al., 2006) of simple-type V1 cells’ responses to optically presented visual stimuli. We expect this simple model will be satisfactory for most users; however using the FPGA platform, users can extend response properties according to their individual needs by adding new code to the model definition, and/or hardware extensions. This model is constructed from an optical front-end (camera lens, filter, optical sensors) and a FPGA development board. It can simulate a tetrode (Gray et al., 1995) recording of up to three independent neurons on four channels of analog outputs. The simulated neurons produce spikes with distinct wave shapes and output differentially weighted sums of these waveforms on each channel. The model can be positioned to observe a physical stimulus screen and be directly connected to a multi-channel experimental recording setup. In response to sinewave grating stimuli, the model exhibits biologically realistic selectivity for orientation and spatial/temporal frequency, with a realistic simple-cell-like space-time receptive field structure. Since the analog output signals can be routed through the entire recording setup, stimulus presentation, data acquisition, and analysis can be easily tested prior to an animal experiment. This model is also suitable for training students on experimental protocols and setup usage, or demonstrating visual cortex neuron behavior in the classroom. The source code and necessary documentation of the

model are provided in the [Supplementary Materials](#). Using these resources, users will be able to build their own FPGA model from commercially available parts, with the option to modify or extend it according to their individual needs.

2. Methods

2.1. Hardware and FPGA programming

The model is composed of two main components: a FPGA development board and an optical front-end. The development board is a Xilinx Spartan-3AN Starter Kit (Xilinx, CA, USA), which includes a Xilinx Spartan-3AN FPGA (XC3S700AN-FG484) chip, a two-channel analog capture circuit, a four-channel analog output circuit, and a variety of connectivity and display options such as a LCD screen, LEDs, slide switches, RS-232 serial ports, and differential I/O connectors. The analog capture circuit consists of a dual-channel programmable scaling pre-amplifier and a 14-bit, 3Msps dual-channel analog-to-digital converter. The analog output circuit consists of a four-channel, 12-bit digital-to-analog converter.

The optical front-end (Fig. 1A) includes a 50 mm SLR camera lens, an optical grating filter (cardboard with two slits) to provide orientation and spatial frequency selectivity, and two optical sensors (T2L12S, TAOS, Texas, USA), one positioned behind each slit. Each optical sensor combines a photodiode and a transimpedance amplifier to provide an analog voltage output that is linearly proportional to input light intensity. All components of the optical front-end are enclosed in a matte black box to prevent stray light reaching the optical sensors.

The Xilinx ISE® WebPack™, free software that runs on a PC (Windows® or Linux), was used to create and compile hardware description code written in VHDL (Very-High-Speed Integrated Circuit Hardware Description Language). The compiled hardware description is then downloaded via a USB port to the FPGA, which can subsequently run “untethered” from the PC.

2.2. Architecture

A functional block diagram of the FPGA model is shown in Fig. 1B. The voltage outputs of the optical sensors are amplified and converted to digital signals by an analog capture circuit on the development board. The digitized sensor signals are differen-

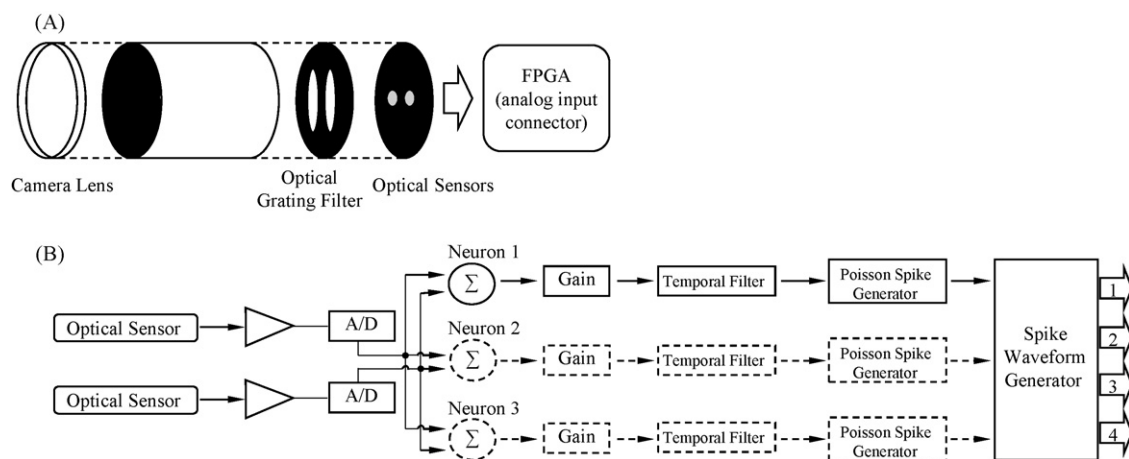


Fig. 1. Architecture for the FPGA model. (A) The optical front-end. It includes a 50 mm SLR camera lens, an optical grating filter to produce spatial frequency and orientation selectivity, and two optical sensors positioned in the image plane of the lens. (B) Functional block diagram of the FPGA model. The model can run in either a one-neuron or a three-neuron mode. For each neuron, the FPGA uses a differential sum of the optical sensor signals to produce orientation and spatial frequency selective membrane potentials. The membrane potential is adjusted by a luminance gain controller to suit different average stimulus luminances, and digitally filtered to provide temporal selectivity. The filtered signal controls the rate parameter of a Poisson Spike Generator, which triggers a spike waveform generator to produce four-channel spike trains that are simulated to mimic signals from a tetrode recording. Dashed lines indicate parts relevant to the three-neuron mode.

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