ELSEVIER

Journal of Neuroscience Methods 168 (2008) 146–150

JOURNAL OF NEUROSCIENCE METHODS

www.elsevier.com/locate/jneumeth

Short communication

A charge-balanced pulse generator for nerve stimulation applications

James Christian Gwilliam*, Kenneth Horch

Department of Bioengineering, University of Utah, 50 S. Central Campus Drive, RM 2480, Salt Lake City, UT 84112-9202, United States

Received 9 May 2007; received in revised form 5 September 2007; accepted 7 September 2007

Abstract

Nerve stimulation typically employs charge-balanced current injection with a delay between the cathodal and anodal phases. Typically these waveforms are produced using a microprocessor. However, once appropriate stimulus parameters are chosen, they tend to remain fixed within an application, making computational power unnecessary. In such cases, it would be advantageous to replace the microprocessor with integrated circuitry and hardware controls for maintaining fixed pulse parameters. We describe here an architecture that generates controllable charge-balanced pulses but requires no computer processing components. The circuitry has been engineered such that minimum size and power consumption can be achieved when fabricated into an IC chip, making it ideal for many long term, portable nerve stimulation devices and applications.

© 2007 Elsevier B.V. All rights reserved.

Keywords: Nerve stimulator; Nerve stimulation; Charge-balanced pulse generator; Nervous system

1. Introduction

To stimulate peripheral (and central) nerve fibers, one typically applies a charge-balanced, biphasic stimulus through implanted electrodes. The first (cathodal) phase of the stimulus depolarizes the cell membrane, thus initiating an action potential. The second (anodal) pulse brings the net charge balance in the electrode to zero. Charge balance is necessary to avoid any adverse long-term effects such as pH shift, ionic charges near the implanted electrodes, and erosion of the electrode material. However, there must be a separation between the cathodal and anodal pulses. If the anodal pulse occurs too quickly after the cathodal pulse, the nerve membrane is re-polarized before threshold is reached, thereby preventing the firing of an action potential. This necessary time in between the biphasic stimulus pulses is referred to as the interphase interval. The magnitude of charge is determined by the product of the amplitude and width of the pulse. Creating a charge-balanced stimulus requires that this product for the anodal pulse be equal to that for the cathodal pulse.

Most nerve stimulation applications are specific in their design requirements and stimulating waveform parameters. As such, many stimulators include a programmable microprocessor for generation of the stimulus waveform (Arabi and Sawan, 1999; Ilic et al., 2004). Examples of applications using microprocessors in the stimulator design include functional activation of denervated muscles (Hofer et al., 2002), control of gastrointestinal motility (Jalilian et al., 2007) and the bladder (Balken et al., 2004), and stimulation of the vagus (Jandial et al., 2004) and common peroneal (Hart et al., 2006) nerves. However, not all stimulating applications require microprocessors to continuously control pulse parameters. In applications where stimulating pulse parameters are fixed (Dhillon and Horch, 2005), or determined for a particular location, such computer processing power is not necessary to re-compute pulse width and amplitude for each stimulus. Instead, a pulse generator constructed entirely from low-powered hardware components, which could consistently generate a user-selected charge-balanced pulse waveform, would eliminate the need for processing components to control pulse parameters. This would increase device portability and minimize power requirements, thus making it valuable in many functional electrical stimulation applications. The creation of such a device was the subject of this work.

2. Methods

Edge-triggered monostable multivibrators (SN74121, Texas Instruments) were used to generate digital pulses. An advantage of edge-triggered technology is that the duration of the trigger

---

* Corresponding author at: 6203-D Pimlico Road, Baltimore, MD 21209, United States. Tel.: +1 801 573 3175; fax: +1 801 966 9954.

E-mail address: jimgwilliam@gmail.com (J.C. Gwilliam).

0165-0270/$ – see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.jneumeth.2007.09.004

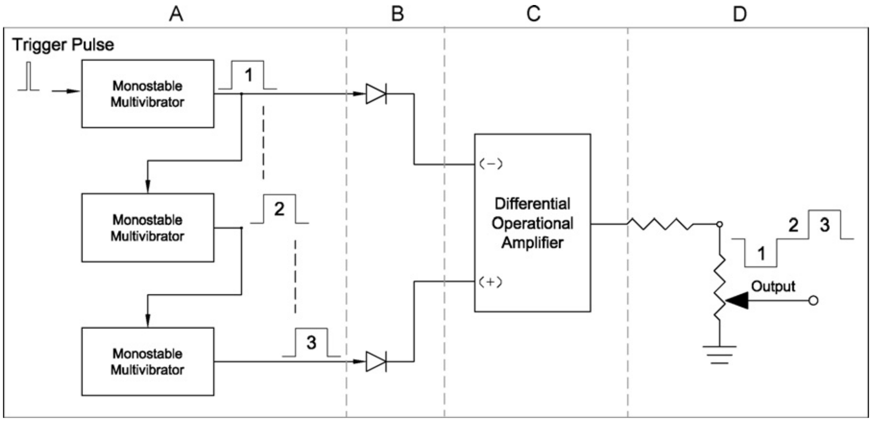

Fig. 1. After being initiated by a trigger pulse, three edge-triggered timing chips placed in series generate timed, digital output pulses (A) to provide controllable pulse widths and an interphase delay. Diodes placed at the output of the first and third multivibrator timing chips (B) remove unwanted low-level voltages, while still conducting the high-level cathodal and anodal pulses. The resulting cathodal and anodal pulses are amplified to saturation, with the cathodal pulse inverted (C). Final output pulse amplitudes are controlled by a voltage divider (D).

stimulus (pulse) is unimportant, so long as it remains shorter than the period between successive trigger stimuli.

Since there are three intervals/durations in the stimulus, three monostable multivibrators were used in series (Fig. 1A) to produce timed, digital output pulses. The input trigger pulse produces an output from the first multivibrator, which serves as the source for the cathodal phase of the stimulus and as the trigger for the second multivibrator. The latter provides the interphase interval and a trigger for the third multivibrator, which provides the anodal phase of the stimulus. The cathodal pulse is fired from the rising edge of the trigger pulse. The interphase interval and anodal pulse are both fired from the falling edges of their input pulses. By using edge-triggered timing chips, the outputs are independent of further transitions of the inputs and are a function only of the timing components used. The timing components, consisting of a resistor and capacitor combination, define the duration (width) for any output pulse. By selecting a constant capacitance value, alterable resistance values achieve the required various output pulse durations. Pulse widths for the cathodal and anodal stimulus phase were varied stepwise and identically by utilizing a two-level ganged rotary switch. Interphase interval duration was controlled using a rotary switch with incremental resistance values.

Specifications for the multivibrators indicated that low-level output voltages could be as high as 0.4 V, instead of the nominal 0 V. This would be problematic for amplification of the signal in later stages of the circuitry, as any non-zero signal, no matter how small, would induce a residual current flow. Therefore, low-level voltages emitted from the multivibrators needed to be blocked, without blocking the intended output pulses. Placing standard forward-biased silicon diodes at the output of the first and third multivibrator timing chips (Fig. 1B) blocked residual voltages when the multivibrators were in their low state, while still conducting the high-level voltages.

The output pulses from multivibrators 1 and 3 were amplified to saturation by a differential amplifier (NTE858M. NTE Electronics) (Fig. 1C), resulting in inversion of the cathodal pulse. One might assume that a simple comparator could more easily be utilized in place of the differential amplifier. However, when the two inputs are at a nominal 0 V, the output of the comparator is unstable and will tend to rail at one extreme or the other. For this reason, a differential amplifier was used and the gain was set high enough to saturate the output during high-level pulses, but low enough to produce 0 V output when the two inputs were zero. Amplifying the pulses to saturation ensures constant output and equal final output pulse amplitudes. The resulting output was fed through a voltage divider (Fig. 1D), ensuring that at maximum and minimum potentiometer position, amplitudes of 10 and 0 V were achieved, respectively. A voltage follower connected to the wiper of the potentiometer (not shown) was used to buffer the output. The schematic for the charge-balanced pulse generator is shown in Fig. 2.

Using diodes to remove low-voltage output creates asymmetrical gain between the cathodal and anodal pulses. This occurs because the basic op amp equations require that the point between D_2 and R_{G2} looks like ground for any signal coming from the output, so the R_{G1}/R_{G2} divider can work properly (Fig. 2). Insertion of diode D_2 prevents the intended voltage division between R_{G1} and R_{G2} from occurring when the diode is reverse biased, limiting the amplifier gain to 1.

Since the desire was to drive the op amp to saturation, and linear gain was not required, the problem was addressed by adding a resistor R_X in between D_2 and R_{G2} so that feedback signals from the op amp output to the inverting input always had a path to ground. R_X was selected to be small enough to allow saturation of both cathodal and anodal pulses, but not so small as to draw excess current through diode 2 (D_2). Trial and error showed that 10.0 kΩ was the largest resistor value that resulted in symmetrical output between the anodal and cathodal pulses.

Standard 120 V ac line power was used to power the stimulator. The circuitry components required ±15 V dc for the NT858M dual op amp and +5 V dc for the SN74121 monostable multivibrator timing chips. A dc power block was used to obtain the ±15 V, and a 7805 voltage regulator (KA7805, Fairchild Semiconductor) was used to derive the +5 V. A 0.2 A fuse was used to protect circuit components. Capacitors were placed in between the +5 V and ground leads of the 7805 voltage regulator to help stabilize the +5 V rail during active signaling.

Download English Version:

https://daneshyari.com/en/article/4336625

Download Persian Version:

https://daneshyari.com/article/4336625

Daneshyari.com