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Realization of current-mirror filters with large time-constants

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ABSTRACT

A novel scheme for realizing large time-constants in analog filters, using current-mirrors as active elements, is introduced in this paper. Instead of employing conventional capacitor multipliers, the proposed concept is based on the realization of very low values of transconductance. This has been achieved through a linear compression of the input signal in order to achieve operation of the core in a reduced bias current. The expansion performed by the output stage preserves the gain of the whole system. The validity of the proposed scheme as well as the offered benefit have been verified through simulation results using the Analog Design Environment of the Cadence software.

1. Introduction

Current-mirrors are attractive cells for performing current-mode analog signal processing. This is originated from their simple structure which provides capability for implementing filters with reduced power dissipation [1]. This is a very important feature, especially in biomedical applications where the battery life of implantable devices should be maximized.

Owing to the low frequency range of the biological signals, the current-mirror would be feasible for biomedical applications only in the case that they are capable for realizing large-time constants. Due to the fact that the formed time-constants are given by the expression $\tau = C/g_m$, where g_m is the small-signal transconductance of the input MOS transistor which is dependent on the level of the bias current I_o, the achievement of large time-constants could be performed by increasing the value of capacitance and/or reducing the value of transconductance through an appropriate adjustment of the bias currents.

With regards to the first solution, capacitance multipliers have been already introduced in [2–4]. The solution in [2] is based on the employment of current-mirror as active element, while in [3,4] the active elements were Operational Transconductance Amplifiers (OTAs) and/or second generation Current Conveyors (CCIIs). Thus, in terms of simplicity the scheme in [2] is the most preferable.

With regards to the second solution, the reduction of transconductance could be achieved through a reduction of the related dc bias current I_o. Taking into account the class-A nature of the current-mirror filters, the level of the input current should be smaller than that of the bias current (i.e. $i_{in} \leq I_o$). Therefore, this solution dramatically limits the range of the input currents which could be successfully handled by the filter.

In order to overcome the aforementioned difficulties, an alternative solution for realizing large time-constants is presented in this paper. According to this, capacitance multipliers have been avoided and a scaling of the transconductance used for realizing the time-constant is performed without restricting the range of the input currents. These have been achieved through the employment of appropriate linear compression and expansion of the input and output currents, respectively. The paper is organized as follows: the proposed scheme is presented in Section 2, while its performance is evaluated and compared with that offered by the conventional topology in Section 3, using the Analog Design Environment of the Cadence software and the Design Kit of the TSMC 180 nm CMOS process.

2. Proposed scheme for realizing large time-constants in current-mirror filters

A typical Functional Block Diagram (FBD) of a current-mode 1st-order lowpass filter is depicted in Fig. 1a. A possible realization using current-mirrors as active elements is demonstrated in Fig. 1b [1] and the ac transfer function is given by (1)

$$\frac{i_{out}}{i_{in}} = \frac{1}{1+\tau \cdot s}. \quad (1)$$

The variable τ in (1) is the time-constant, given by

$$\tau = \frac{C}{g_{m,Mn1}}, \quad (2)$$

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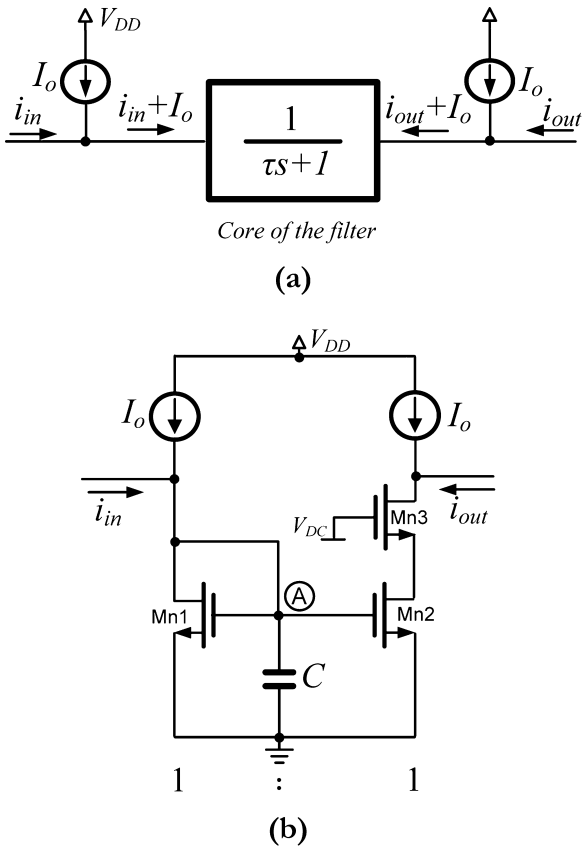

Fig. 1. Typical 1st-order filter using current-mirror (a) Functional Block Diagram (FBD) representation, and (b) typical circuitry.

where $g_{m,Mn1}$ is the small-signal transconductance parameter of M_{n1}.

Assuming operation of the transistors in the subthreshold region, the expression in (2) takes the form in (3)

$$\tau = \frac{nV_T C}{I_o}, \tag{3}$$

where n is the subthreshold slope factor ($1 < n < 2$), V_T the thermal voltage (≅26 mV at 27 °C), and I_o the bias current.

According to (3), large time-constants could be realized by increasing the value of capacitor through the employment of a capacitance multiplier and/or reducing the value of transconductance of M_{n1} by a factor K.

The capacitance scaling introduced in [2] is depicted in Fig. 2, where a multiplication of the capacitor value by a factor $(K+1)$ is realized. The corresponding filter topology suitable for realizing large time-constants would be more complicated than that in Fig. 1b, because the capacitor would be substituted by the scheme in Fig. 2. In addition, the dc power dissipation of the filter in Fig. 1 is 2 $V_{DD}I_o$, while the corresponding value for the scheme with capacitor scaling would be significantly increased to a level $(3+K)V_{DD}I_o$.

The reduction of the value of transconductance g_m through the reduction of the value of I_o is not a practical solution, because this leads to a reduction of the maximum input current which could be successfully handled by the filter.

The proposed solution for lowering the transconductance without affecting the range of the input current is demonstrated, at FBD level, in Fig. 3a. The introduced concept is the linear counterpart of the concept of companding filters where the instantaneous (i.e. the sum of dc and ac components) input current is non-linearly

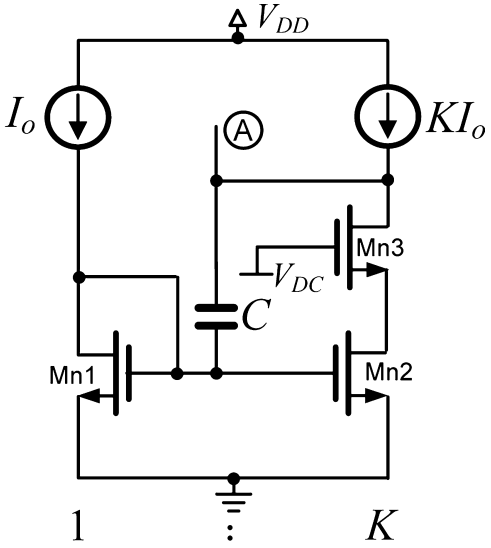

Fig. 2. Capacitor multiplier introduced in [2].

compressed into a voltage and after its procession is (non-linearly) expanded into a linear current. The realization of large-time constants in the companding filters has been introduced in [5], where appropriate modifications in the bias of current dividers have been performed. Companding filters suffer from increased circuit complexity and, therefore, from increased power dissipation, making the current-mirror filters attractive candidates for realizing ultra-low power filters suitable for handling extremely low frequency signals.

The circuitry that implements the FBD in Fig. 3a is given in Fig. 3b. The current that feeds transistor M_{p1} is $i_{in}+I_o$ while, due to the current mirror formed by transistors $M_{p1}-M_{p2}$, the current in transistor M_{n1} will be equal to $(i_{in}+I_o)/K$. Thus, a linear compression of the instantaneous value of the input current is performed. Taking into account that both the dc (I_o) and ac (i_{in}) components of the input current are compressed then, according to (3), the value of transconductance of M_{n1} is decreased by a factor K. Therefore, according to (3) the realized value of time-constant is increased by the same factor. In order to achieve a low-frequency gain equal to one, the output current of the current-mirror $M_{n1}-M_{n2}$ is scaled by a factor K and this is obtained through an appropriate choice of the aspect ratio of M_{n2}. Thus, transistor M_{n2} performs a linear expansion of the output current in order to preserve the gain of the whole filter.

It should be also mentioned at this point that the amplitude range of the input current is determined by the level of dc bias current (I_o) and, therefore, there is not affected by the proposed solution. In other words, an orthogonal adjustment between the achieved scaling factor and the level of the maximum current that could be handled by the filter is achieved and this is very important from the design flexibility point of view.

Inspecting the topologies in Figs. 1b and 3b it is readily obtained that the realization of a large value of time-constant is achieved through the addition of just one current mirror (i.e. two transistors). The total power dissipation has been increased from its initial value 2 $V_{DD}I_o$ to $[2+(1/K)]V_{DD}I_o$. Taking into account that the solution derived using the extra block in Fig. 2 leads to a configuration with an extra number of five transistors and a total power dissipation $(3+K)V_{DD}I_o$ it is readily concluded that the proposed solution is the most attractive in terms of circuit complexity and power dissipation.