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Wide-bandwidth CFOA with high CMRR performance

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ABSTRACT

In this paper the authors analyze the conventional current-feedback operational amplifier (CFOA) in terms of common-mode-rejection ratio (CMRR) performance, and having identified the mechanism primarily responsible for the CMRR, they propose two new architecture CFOAs. These new CFOAs are further developed, and modified to provide improved bandwidth, AC gain accuracy and high CMRR performance. The key features of the two proposed new CFOAs are the designs of the internal voltage followers which have two separate biasing currents with a similar dynamic architecture to that of the conventional CFOA. The magnitude of one bias current determines the value of the maximum CMRR, and the second can be used to maximize bandwidth.

1. Introduction

In electronic circuit design, there are many occasions where a general-purpose voltage operational amplifier (VOA) is useful [1]. If the application calls for differential inputs, high input impedance, low output impedance, high common-mode rejection ratio (CMRR), and low input referred offset voltage, the VOA provides a basic topology for achieving these requirements [2]. Unfortunately it has inherent limitations in both the gain-bandwidth trade-off and slew-rate [3]. Typically, the gain-bandwidth product is a constant and the slew-rate is limited to a maximum value determined by input stage bias current. The slew-rate limitations of the VOA are overcome in relatively new architecture op-amps, commonly referred to as the current-feedback op-amp (CFOA) [4,5]. CFOAs have been around approximately 30 years, but their popularity has increased only in the last 10 years. CFOAs are receiving increasing attention as basic building blocks in analogue system design, and they are now recognized for their excellent performance in high speed and high slew-rate analogue signal processing applications [6]. Despite excellent high frequency and high speed performance, CFOAs generally exhibit poorer common-mode rejection (CMRR) properties, compared with their voltage-mode counterpart, which limits their utility [7].

Electronics manufacturers and telecommunications systems engineers are endeavouring to achieve the highest specifications for a voltage follower [8]. The differential pair is inherently good in providing high CMRR. However, applications such as DAC/ADC buffers, high-quality video front-end, RF/IF drivers, ATE pin drivers, video-line drivers, some medical applications and video switchers showed that having high CMRR, and low DC voltage offset was not enough [9,10]. The need for a high-slew-rate voltage follower with a high bandwidth, and low settling-time is desirable for such applications [11,12]. In this paper the authors analyze the conventional CFOA and identify the main reasons for the poor CMRR performance. These results were used to inform the development of a new architecture design which addresses the shortcomings in terms of CMRR and gain accuracy. The two new voltage followers proposed in this paper maintain both high slew-rate and good CMRR performance.

2. Analysis of differential-mode operation

A detailed analysis of the input stage is presented in this section to obtain a clear understanding of the operation of the amplifier and gain insight into ways that the circuit can be modified to improve its performance. A simplified schematic of the standard CFOA architecture is shown in Fig. 1 where the non-inverting and inverting nodes are connected to a differential input signal V_2 and V_1 respectively. The positive differential input signals are $V_2 = +(V_{in}/2)$ and the negative differential input signal is $V_1 = -(V_{in}/2)$. When the positive signal (V_2) is applied, the voltage at the base of Q_1 will rise, and the voltage at the emitter of Q_1 will fall due to the negative signal (V_1), increasing V_{BE1} of Q_1 and resulting in an increase of I_{C1}. Similarly, V_{BE2} of Q_2 decreases and I_{C2} reduces. Under small-signal the collector current I_{C1} of Q_1 will rise by ΔI and, similarly, the collector current I_{C2} of Q_2 will

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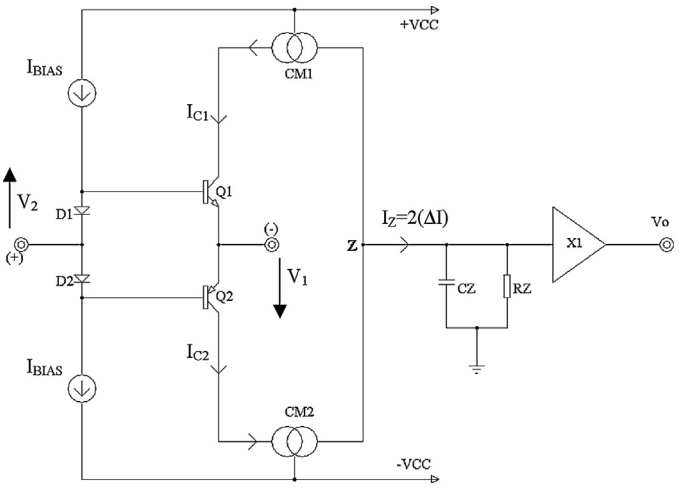

Fig. 1. Simplified schematic of a standard CFOA.

fall by ΔI [13]. Currents I_{C1} and I_{C2} are then mirrored by CM1 and CM2 to a high impedance gain-node (Z), where they subtract, giving a total signal current $I_Z = 2\Delta I$, resulting in an output voltage $V_{out} = 2\Delta I Z_Z$.

Transistors Q_1 and Q_2 are configured as a class-AB complementary-pair stage. The operating point of these transistors is in the active region and class-AB with the DC current set by the bias network comprising the two diodes D_1 and D_2 and the two current sources, I_{BIAS}.

Fig. 2 shows the small-signal differential-mode half circuit, which can be analyzed to predict the circuit behaviour. $V_d = V_2 - V_1$. The output current $i_{C1} = i_{out(dm)}$ is given by

$$i_{C1} = g_m V_{BE1} + \frac{v_d}{2r_{ce1}} \tag{1}$$

Since $V_{BE} \approx v_d$ and r_{ce1} is very large compared with $1/g_m$, Eq. (1) can be reduced to

$$g_{Tdm} \approx \frac{2i_{C1}}{v_d} = 2g_m \approx \frac{2}{r_e} \approx \frac{2I_{CQ}}{V_T} \tag{2}$$

where g_{Tdm} is the transconductance of the differential-mode operation, g_m is the transconductance of one particular transistor at a time in the input class-AB complementary-pair, I_{CQ} is the dc bias current, and V_T is the thermal-voltage. Thus the differential-mode gain, A_{dm}, of the CFOA is approximately

$$A_{dm} = \frac{2i_{C1}Z_Z}{v_d} = g_{Tdm}Z_Z, \tag{3}$$

where Z_Z is the high impedance of the gain-node of the CFOA.

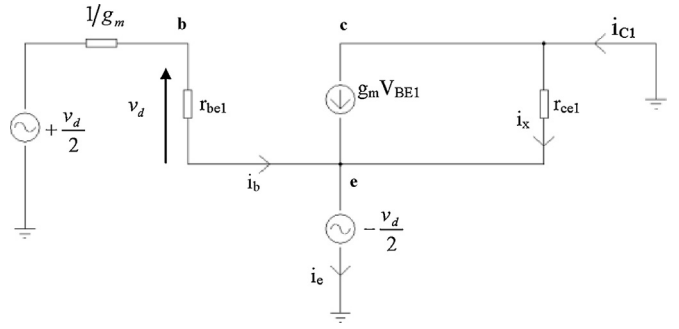

Fig. 2. Small-signal differential-mode half circuit.

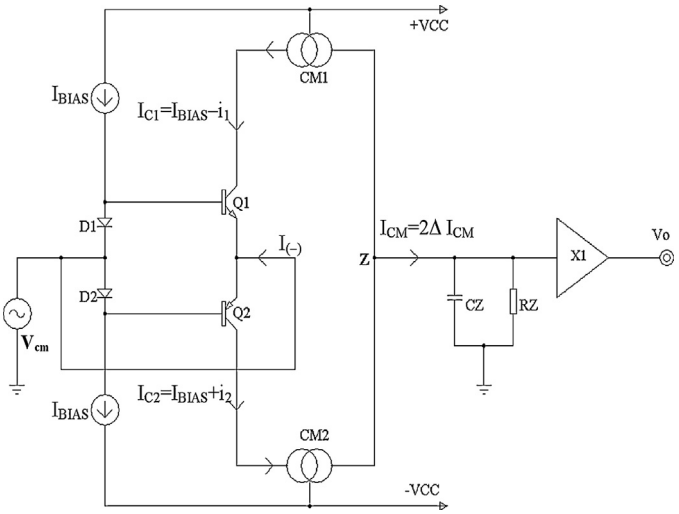

Fig. 3. Circuit schematic of the CFOA with a common-mode input signal, V_{cm}.

3. Analysis of common-mode operation

The input stage of the CFOA is the main factor in determining the CMRR performance of the CFOA [9,13]. A further study has been made to investigate the parameter that has a direct responsibility towards the common-mode operation, in order to fully understand the inner working of the CFOA, when a common-mode signal is applied to its input. It has been reported that the drawback of the CMRR performance of the CFOA is due to the output impedances of transistors in the input stage [13–15]. The currents i_1 and i_2 which flow through the output impedance of Q_1 and Q_2, respectively, as a direct result of the common-mode input voltage V_{cm}, are given by

$$i_1 = \frac{V_{cm}}{r_{ce1}} \quad \text{and} \quad i_2 = \frac{V_{cm}}{r_{ce2}}. \tag{4}$$

These currents are then mirrored to a high impedance gain-node (Z), where they add algebraically. Thus a high common-mode voltage gain is generated, and a low value of the CMRR is produced, normally in the region of 50 dB.

Fig. 3 shows a circuit schematic of the CFOA with a common-mode input signal. Applying a positive common-mode input signal decreases the value of V_{CB} of Q_1, and as the Early voltage of this transistor is finite it results in a decrease in the collector current I_{C1} of Q_1 by an amount ΔI_{CM}. Furthermore, the positive common-mode input voltage will cause the value of V_{CB} of Q_2 to rise and, thus, the collector current I_{C2} of Q_2 to increase by the same amount [13,15].

Hence, when the collector currents of Q_1 and Q_2 are mirrored by CM1 and CM2 to a high impedance gain-node (Z), the net current into the Z-node is

$$I_Z \approx I_{C2} - I_{C1} = (\Delta I_{CM}) - (-\Delta I_{CM}) = 2\Delta I_{CM} \tag{5}$$

Since $I_{C1} \approx I_{E1}$ and $I_{C1} \approx I_{E1}$, then $I_{(-)} = I_{C2} - I_{C1}$, where $I_{(-)}$ is the inverting node input current. Thus,

$$I_Z \approx I_{(-)} \approx I_{C2} - I_{C1} = 2\Delta I_{CM} \tag{6}$$

To obtain a better understanding, the class AB bias voltage follower (shown in Fig. 3) was analyzed using small-signal modelling.

Fig. 4 shows the small-signal equivalent circuit for the input stage of the CFOA driven by an input common-mode voltage signal. Since $1/g_m$, $r_{in(CM1)}$ and $r_{in(CM2)}$ are small, and the bases of Q_1 and Q_2 are connected together, there will be negligible signal voltage across the base to emitter terminals of these two input transistors in Fig. 4 when a common-mode input voltage is applied to the circuit. Hence, both $g_{m1}V_{BE1}$ and $g_{m2}V_{BE2}$ signal current generators are