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Tutorial paper

OTA based frequency tuning system with reduced effect of DC offsets

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ABSTRACT

An on-line tuning system based on the master–slave technique is proposed in this paper. Each stage of the system is realized by employing only operational transconductance amplifiers (OTAs). The most significant advantage of the introduced topology is the reduction of the influence of the dc offset terms which are critical about the performance of such systems. In addition, an attractive benefit is the suitability for implementing the resulted configurations in both integrated and discrete-component forms using only the same type of active element. The validation of the proposed topology is achieved through simulation and experimental results.

1. Introduction

OTAs are very attractive elements used for realizing active filters. An advantage of this kind of filters is that OTA is a well established element in the literature, offering attractive benefits, like ability for operation at high frequencies, simplicity in the design process, electronic tuning [1–3], and accessibility to commercial elements. Continuous time filters with electronic frequency tuning are used in a wide range of applications including instrumentation, control, and communication systems. The electronic tuning offers compensation of the variations of the cutoff frequency caused by parameter deviations of the passive and/or the active elements. In many applications a high precision of the cutoff frequency is critical and, thus, a simple electronic tuning is not enough. In these cases an automatic frequency tuning system [4,5] is required in order to guarantee that the filter will be automatically kept on its nominal cutoff frequency.

Typically, the operation of an automatic tuning system is based on the comparison of an electrical signal of the system with a reference signal and, as a next step, on the generation of a feedback control signal [6]. Simple tuning topologies offer attractive benefits, like reduced number of active and passive elements, reduced power consumption, and rapid design procedure; on the other hand, they suffer from reduced accuracy that could be improved by employing more complicated structures.

Some of the proposed techniques are based on direct [5] or indirect tuning [7,8], and digital [9] or analog control [10]. Phase locked loops (PLL), voltage controlled oscillators (VCO), and voltage controlled filters (VCF) are often employed in the analog control systems but they need complicated circuits to overcome their drawbacks [11].

The master–slave technique that compares the signal amplitudes of two different paths is often used and belongs to the category of the indirect tuning.

Topologies based on this concept have been already published in [12,13], where OTAs have been employed as active elements. A drawback of these topologies is the effect of the dc offsets caused by the employed OTAs.

In order to reduce the above imperfection, an automatic tuning system based on the master–slave technique, realized by employing only OTAs is proposed in this paper. As in [12,13], the system is used to tune a slave filter using a Gm-C integrator as a master filter. Compared with [13] the proposed topology minimizes the influence of the dc offsets that are critical in such systems [13]. The main advantage of the proposed method compared with those proposed in [12,13] is that the main tuning system as well as the filter can be both implemented by using only OTAs. Preliminary results about this concept have been initially published in [14]. These are now further enhanced including detailed mathematical analysis and, also, experimental results. The paper is organized as follows: in Section 2 the introduced system is analytically described, while in Section 3 the derived simulation results are given. Also, in Section 3, experimental results, obtained by employing the commercially available LM13700 OTA validate the operation of the proposed method.

2. The proposed tuning system

A tuning system based on the master–slave technique and on the envelope locked loop method is presented in [13]. This topology improves that proposed in [12], with regards to the dc

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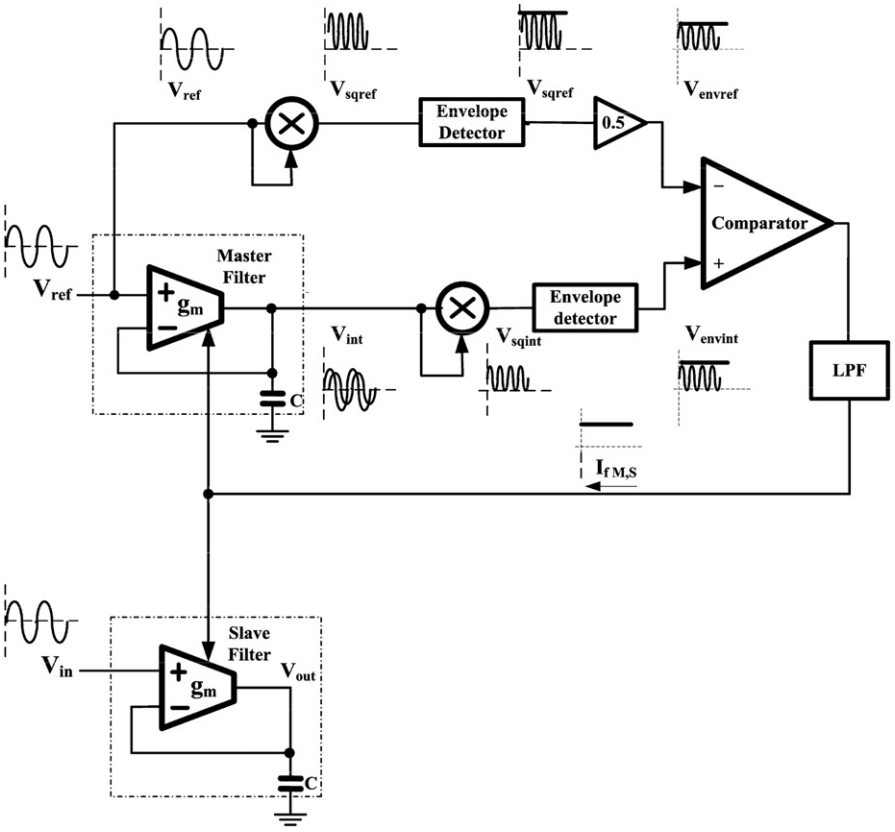

Fig. 1. Block diagram representation of the topology proposed in [13].

offset caused by the OTAs of the master integrator. If these OTAs have a finite dc offset, the output of the master integrator can be easily saturated. In [13] a degenerated integrator is used as the master filter in order to eliminate the problem of the dc offsets. Different dc offsets in the two paths can cause the comparator to lock the loop to a fault value. Therefore the equality of the dc offsets is critical for the correct operation of the loop. The topology presented in [13] is shown in block diagram in Fig. 1. It employs four basic blocks: a master integrator, a squarer circuit, an envelope detector, a comparator with a lowpass filter and a voltage attenuating block. However, in that topology different dc offsets can be produced at the outputs of the two multipliers because the one path introduces a dc offset from the reference signal while the other path introduces a completely different offset from the master integrator.

A way for reducing the influence of the dc offsets is to make them equal each other at the input of the comparator. Thus, an effort must be given for equalizing the effects of the dc offsets. In this way similar dc offsets in both paths finally can be canceled by the comparator at the nominal frequency. Although the topology in [13] improves the behavior of [12] it still causes a dc drift at the expected value of the feedback current and consequently, generates a frequency shift. This can be explained by the unbalanced circuitry between the two paths that the external sinusoidal reference signal V_{ref} follows towards the comparator input.

A possible realization of the topology in Fig. 1, using only OTAs, is that shown in Fig. 2. It will be used for a detailed study regarding the effect of the dc offsets on the circuit. In order to simplify the analysis, we can assume that all OTAs are identical and they produce a standard dc current offset I_{offset}. Setting I_{out} as the total output current, V_+ and V_- as the positive and negative inputs and g_m as the transconductance of an OTA, I_{out} can be given as

$$I_{out} = I_{offset} + g_m(V_+ - V_-) \tag{1}$$

The master filter is realized as a typical first order Gm-C integrator with one OTA, as is shown in Fig. 2. The voltage V_{ref} is a sinusoidal signal of the form,

$$V_{ref} = A \cdot \sin(\omega_{ref} \cdot t) \tag{2}$$

where $\omega_{ref} = 2\pi f_{ref}$ is the nominal cutoff frequency. If the time constant τ is equal to $1/\omega_{ref}$, the output signal of the master integrator, for the ideal case where there is not any dc offset, is defined as

$$V_{int} = \frac{A}{\sqrt{2}} \cdot \sin(\omega_{ref} \cdot t - \pi/4) \tag{3}$$

If τ is larger than $1/\omega_{ref}$ the gain is smaller than $A/\sqrt{2}$ and vice versa. Therefore, by controlling the gain of the integrator in order to be equal to $V_{int} = V_{ref}/\sqrt{2}$, we can control the time constant to be $1/\omega_{ref}$.

Taking into account the dc offsets, the voltage V_{int} is expressed after a routine algebraic analysis, as,

$$V_{\text{int}} = \frac{I_{offset} + g_m \cdot V_{ref}}{g_m + sC_M} \tag{4}$$

where C_M is the capacitor of the master filter.

At cutoff frequency, (4) can be expressed as

$$V_{int} = \frac{1}{\sqrt{2}} \cdot V_{ref} + \frac{I_{offset}}{g_m\sqrt{2}} \tag{5}$$

According to Fig. 2, the squarer is realized by a multiplier where its inputs are short-circuited. It consists of three OTAs and has been selected among others, because it minimizes the dc