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A divider-less, high speed and wide locking range phase locked loop

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ABSTRACT

A high performance, high frequency phase-locked loop (PLL), based on a divider-less structure is presented in this paper. This PLL includes an open-loop phase frequency detector (PFD) and a bulk driven charge pump which is designed by utilizing a 0.18 μm CMOS process with a 1.8 V power supply. The proposed PLL has a locking range frequency of 2.5–7.3 GHz. The rms and peak-to-peak jitters of this PLL at 5 GHz are 3.21 and 0.88 ps respectively. The total power consumption is approximately 13.4 mW.

1. Introduction

The phase-locked loop and the delay-locked loop (DLL) play the role of generating a clock signal that is usually a multiple of a reference clock and is synchronized with the reference clock in phase. They are widely used in many applications including frequency synthesis, phase/frequency modulation and clock data recovery.

In the PLL and DLL, the phase frequency detector is often considered as the bottleneck which limits the data rates that can be achieved by the PLL.

In conventional PLLs, the PFDs cannot detect the phase differences between reference and feedback clocks in high frequencies. To overcome this issue, for high frequency applications, a frequency divider circuit is used in the feedback path of the PLL. Therefore, the clock frequency is reduced which allows the PFD to follow the clock frequency. However, adding the divider circuit extremely increases the overall jitter of the PLL. Thus, a high frequency PFD can improve the low noise behavior of a PLL by omitting the divider circuit [1].

Another important component of the PLL is charge pump circuit. The charge pump is usually used in combination with a PFD supporting a wide output voltage range. The task of the charge pump is to convert the output signal of the PFD into a precise quantity of current. In practice, non-idealities of the charge pump decrease the performance of the entire loop. Current mismatch in the charge pump causes phase offset and reference spurs while the variation of the output current amplitude due to the change of the output voltage will result in variation of the loop bandwidth. The simultaneous increase in current matching and control voltage range cause an increase in the locking range frequency of the PLL.

1.1. Proposed PFD

The proposed PFD is designed using an open-loop structure. Unlike conventional PFDs, with closed-loop structures, the open-loop structure does not make a reset signal in the circuit. As mentioned in [2,3] the reset signal causes many problems in the PFD circuits such as creating a dead zone and a blind zone. Previous works have attempted to modify the reset signal. For example, in [2] the blind zone is reduced by changing the pulse width. However, another issue that arises from the reset signal is the missing edge. With this problem, some of the rising edges can be missed in the detection when the edges signal overlaps with the reset signal internally made in the PFD [4,5].

The proposed circuit eliminates the feedback path in closed-loop structure and creates an open-loop circuit. Therefore, high speed performance can be attained without the issue of the reset signal.

In order to design the proposed PFD, two simple, symmetrical and discrete circuits have been used. One of them has an UP signal production responsibility and another produces a DOWN signal production responsibility. The main idea of this phase detector is based on Fig. 1 which is investigated in both lag and lead of signals A to B. In Fig. 1(b) A leads B. A rising transition on A leads to the turning on of the M1 transistor. Therefore, the UP output node will be set to the high value. The UP output node remains in this state until B signal reaches its rising edge, at which point M2 is turned on and makes the UP signal zero. It must be noted that M2 size is chosen to be larger than M1, so that M2 will have more dominant

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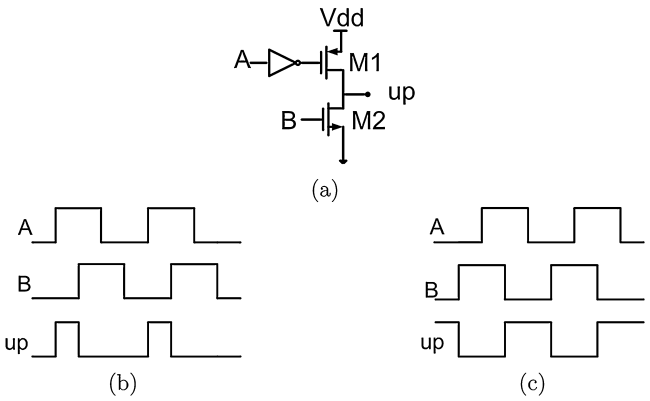

Fig. 1. (a) Primary design, (b) A leads B, (c) A lags B.

Table 1
Different states of PFD in (a) lead and (b) lag.

A	B	UP
(a)		
1	1	0
0	1	0
0	0	Previous state
1	0	1

A	B	UP
(b)		
1	1	0
1	0	1 (Expected to be 0)
0	0	Previous state
0	1	0

effect. This means that the output signal would be zero if both transistors were on. In order to determine the output low voltage as V_{OL}, the circuit design is started by writing the relevant equation. Note that in the case of (A = 1, B = 1) state, M2 transistor is operating in the linear region and the output voltage is equal to V_{OL}.

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left[(V_{dd}-V_{thn})V_{OL}-\frac{1}{2}V_{OL}^2\right] = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p(V_{dd}-V_{thp})^2,\ \mu_n C_{ox}=3\mu_p C_{ox} \quad (1)$$

Assuming V_{OL} = 0.2 V and solving the above equation, the following equation is obtained.

$$\left(\frac{W}{L}\right)_n \cong \left(\frac{W}{L}\right)_p \quad (2)$$

In the worst case, it can be assumed that the (A = 1 and B = 1) state is occurring during 50% of the operating time (however in the modified circuit, which is mentioned later, due to the added delay circuits, this time will be less than 50%). The average DC power consumption of the proposed PFD can be estimated as follows:

$$P_{DC}(average)=\frac{1}{2}[V_{dd}(I_{DM1sat}=I_{DM2linear})] \quad (3)$$

By choosing I_{DM1sat} = 120 μA, the average DC power consumption of the above circuit is estimated as 0.1 mW.

As it is observed, in Fig. 1(b), UP signal is made well, but as it is shown in Fig. 1(c) if signal A is lagging, this circuit alone will not be responsive. For example, when A is "1" and B is "0", UP signal will become high and remain in this state, as long as "B" is "0". While it should have a DC signal with zero amplitude in UP, until A is lag. For better evaluation, the different states of this circuit in lag and lead are shown in Table 1.

When A lags B (Table 1(b)), the (A = 1 and B = 0) state will occur after the (A = 1 and B = 1) state, while in the case of A leading B (Table 1(a)) it occurs after the (A = 0 and B = 0) state. Considering this difference, the circuit was modified as shown in Fig. 2(a). Its corresponding waveforms in ideal state are shown in Fig. 3. In this circuit, when both A and B signals are set to the high value, the lag-comp signal will be set to a low value and it will remain unchanged for the (A = 1 and B = 0) state, which will happen immediately afterward. Lag-comp output becomes inverted and turns on M6, so that the UP output will be set to a low value. It should be noted that M6 size is similar to M2. In the lead state, this circuit does not play an effective role in the output. In fact, only M1 and M2 specify circuit speed with consideration that the high path is passed across the transistor M1 and the low path, through M2, so that the circuit speed will be too high. Furthermore, the effect of the M6 transistor is added to the effect of the M2 transistor to pull down the output. Therefore, they have more dominant effect in the (A = 1 and B = 1) state. To make the DOWN signal, a similar procedure is followed (Fig. 2(b)).

The speed and accuracy will be improved by using this circuit. But the proposed PFD still has a problem. This problem is caused by the precharging time of the internal parasitic capacitances of MOSFETs. When the input phase difference is very small, due to a finite rise and fall time, resulting from the capacitance seen at UP and DN nodes and as shown in Fig. 4, the pulse may not find enough time to reach a logical level. These results in the failure of the charge

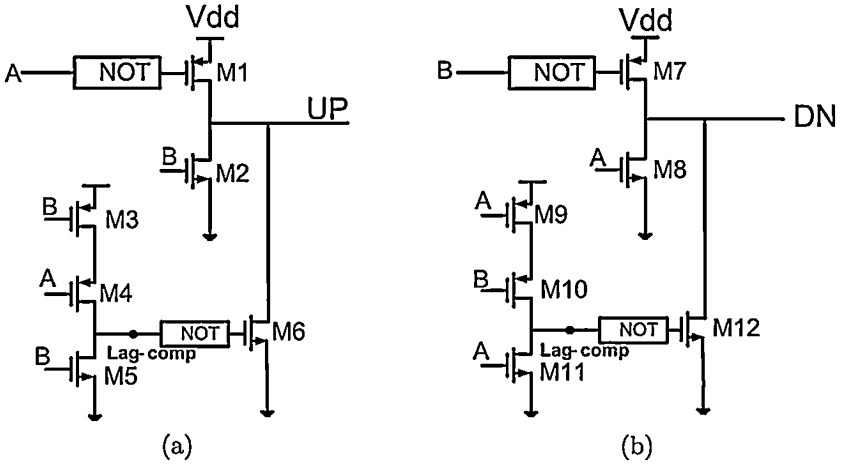

Fig. 2. Proposed PFD (a) up signal, (b) down signal.