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# A broadband Doherty power amplifier with harmonic suppression

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ABSTRACT

In this paper, the design and implementation of the broadband, Doherty power amplifier (DPA) with 2nd and 3rd harmonics suppression, with theoretical analysis is presented. In the proposed structure a novel harmonic suppressed Wilkinson power divider used in DPA, which results in harmonic suppression with high level of attenuation. Moreover the proposed DPA has major advantages in terms of the linearity and works on a wideband frequency range (2.1–2.7 GHz) with minimum 40% drain efficiency (DE). The linearity of the proposed DPA is increased extremely, which significant improvement (7 dBm) is achieved from the main amplifier. In the proposed DPA, the main and the auxiliary amplifiers are implemented using Class-AB and Class-C topology respectively with equal MRF6S27015N MOTOROLA transistors in LDMOS technology.



## 1. Introduction

Nowadays, the rapidly rising power consumption has been occurred by the extensive use of spectrum-efficient modulation techniques, the increasing demand for higher data rates and the growing number of wireless communications users. The energy efficiency of base stations should be constantly improved in order to reduce the power loss. Significant energy savings can be achieved by improving the efficiency of the power amplifier (PA) of RF transmitters used in the base station [1]. Different techniques have been proposed to increase the efficiency of power amplifiers. Envelope elimination and restoration (EER) [2], envelope tracking (ET) [3], Doherty amplifiers [4] and varactor-based dynamic load modulation [5] are the most common techniques being proposed. The ease of configuration and the circuit simplicity give the Doherty power amplifier (DPA) many advantages over the other techniques. In DPA, high average efficiency and high linearity are achieved by dynamically adapting the PA load impedance to keep the amplifier in compression during modulation [4–7].

The Doherty amplifier is considered as a solution to enhance the efficiency and linearization [8,9]. Several approaches have been reported recently to improve linearity [10,11] and wide operation frequency range of the DPAs [12–21].

Recently harmonic control circuit is used for harmonic suppression in class-F and class-E PAs [22–24] for efficiency improvement, which in these classes harmonic control circuit is the most important block in the power amplifiers design [22]. But so far a few Doherty power amplifiers with harmonic suppression have been reported. In [25,26] harmonic suppression has been obtained with defected ground structure (DGS) and lumped reactive components in DPAs. Unfortunately, these methods require either backside etching or additional lumped reactive element, which is undesirable for low-cost and mass production environment [27].

In this paper, a novel Doherty power amplifier with wide operating frequency band, high linearity and harmonic suppression is proposed, where a miniaturized harmonic suppressed Wilkinson power divider is used in the DPA structure, which results in 2nd and 3rd harmonics suppression with high level of attenuation.

## 2. Design process

The basic structure and operation principle of DPAs discussed in this section briefly. The schematic diagram of the conventional DPA is shown in the Fig. 1. The conventional DPA is composed of main and auxiliary power amplifiers. In general, the main amplifier biased for class AB operation, while the auxiliary amplifier has a class C or B bias point to use its low gain at a lower power level [28,29], in the proposed DPA the main and auxiliary amplifier are biased in class AB and C respectively. The main and auxiliary amplifiers are combined through the quarter-wave transmission line in order to modulate the load impedance of the main amplifier through the current supplied by the auxiliary amplifier into the external load. Other parts of the proposed DPA are an impedance transfer network (ITN), a power divider and matching networks, which will be described in the next sections. In the Fig. 1, $Z_M$ and $Z_A$ are the loads seen by the Main and Auxiliary amplifiers.

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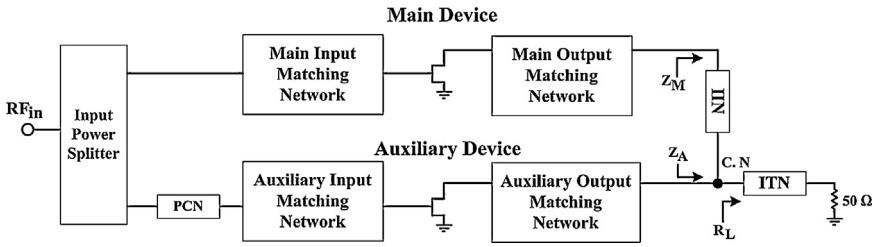


**Fig. 1.** Conventional DPA topology.

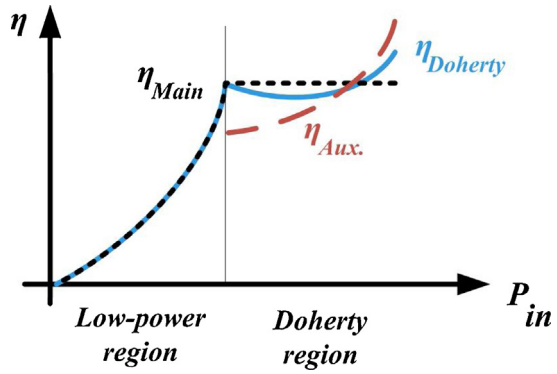


**Fig. 2.** Theoretical efficiency behavior of DPA.

### 2.1. The Doherty amplifier behavioral analysis

The DPA has two operating conditions as shown in Fig. 2. Low-power region, where only the main device is on and the Auxiliary is kept off and Doherty region, which both devices are active [30,31].

The analysis of a DPA starts from the analysis of the current waveforms imposed by the two active devices, according to their biasing level [31]. More in detail, assuming a simplified current source model for the active device, with a constant transconductance ($g_m$) characteristic, a truncated sinusoidal wave shaping can be considered.

#### 2.1.1. Analysis in the low power region

In the low power region, only the main device is operating, and the DPA behaves as a typical Class AB amplifier. The corresponding scheme to be analyzed is shown in Fig. 3. The DPA external load $R_L$ to be selected to assure the maximum drain voltage swing to the main device. Due to simplicity, a maximum voltage swing equal to $V_{Main} = V_{DD} - V_K$, where, $V_{DD}$ is the drain bias voltage and $V_K$, is the device knee voltage, which assumed to be the same for both main and auxiliary devices.

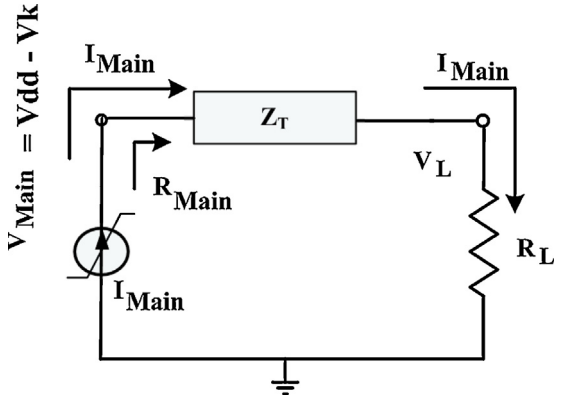


**Fig. 3.** Doherty scheme to be analyzed in the low power region.

By using the quarter-wave constitutional relationship, the impedance seen by the Main device up to the break condition is given by [32]:

$$R_{Main} = \frac{Z_T^2}{R_L} \tag{1}$$

$$\alpha = \frac{P_{out,main,break}}{P_{out,main,max}} \tag{2}$$

$$R_{Main}(x_{brak}) = 2\frac{V_{DD} - V_K}{I_{Max,Main}} \cdot \frac{2}{\pi} \cdot \frac{1 - \cos(\theta_{AB})}{\theta_{AB} - \sin(\theta_{AB})} \tag{3}$$

where the $\theta_{AB}$ is the value of the current conduction angle at the end of the low power region.

#### 2.1.2. Analysis in the Doherty region

In the Doherty region, the scheme to be analyzed is shown in Fig. 4, which both devices are active. The main device can be assumed to behave as a constant voltage source, whose amplitude can be assumed $V_{Main} = V_{DD} - V_K$.

$$V_L(X_{brak}) = \alpha.(V_{DD} - V_K) \tag{4}$$

$$R_L = \frac{\alpha/(V_{DD} - V_K)}{I_{1main}(\theta_{AB})} = \alpha^2.R_{Main(x_{break})} \tag{5}$$

The overall DPA relevant features, such as the output power, the DC power supplied, and the efficiency respectively, given by the following equations:

$$\begin{aligned} P_{out,Main} &= \frac{1}{2}(V_{DD} - V_K).I_{Main} \\ P_{dc,Main} &= V_{DD}.I_{dc,Main} \\ \eta_{Main} &= (P_{out,Main})/(P_{dc,Main}) \end{aligned} \tag{6}$$

$$\begin{aligned} P_{out,Aux} &= \frac{1}{2}V_L.I_{Aux} \\ P_{dc,Aux} &= V_{DD}.I_{dc,Aux} \\ \eta_{Aux} &= (P_{out,Aux})/(P_{dc,Aux}) \end{aligned} \tag{7}$$

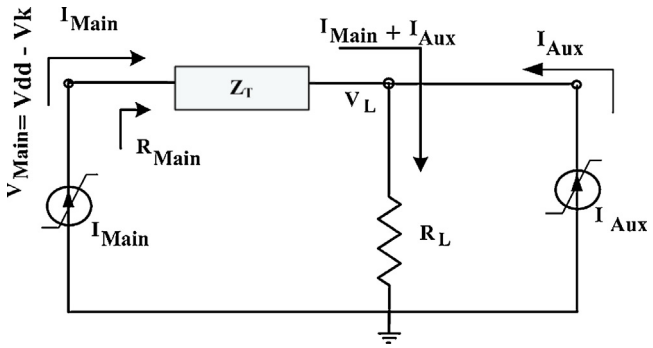


**Fig. 4.** Doherty scheme to be analyzed in Doherty region.