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# Bandwidth enhancement in delta sigma modulator transmitter using low complexity time-interleaved parallel delta sigma modulator

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ABSTRACT

In this paper, the bandwidth of the delta sigma modulator (DSM)-transmitter is improved using low complexity time-interleaved DSM. The high clock speed requirement of DSM is the main limitation to increase the signal bandwidth in DSM-transmitter. In this research, the bandwidth of DSM-transmitter is increased four times by using low complexity four-branch time-interleaved parallel DSM without the need for increasing clock speed. This low complexity parallel DSM is designed based on polyphase implementation technique. Then, the transmitter architecture is simulated using MATLAB simulink and Advanced Design System (ADS). For this simulation, the uplink long-term evolution (LTE) signal with different bandwidths of up to 7.68 MHz is used. The simulation shows that by using four-branch time-interleaved parallel DSM in transmitter architecture for 7.68 MHz LTE signal with oversampling ratio (OSR) of 16, the signal to noise and distortion ratio (SNDR) is about 41 dB with the clock speed of only 30.72 MHz. This is four times lower than the required clock speed of the conventional transmitter to achieve the same SNDR.



## 1. Introduction

Modern communication standards like long-term evolution (LTE) are using advanced spectrum efficient modulation schemes in order to reach high data throughputs. As a result, the peak to average power ratio (PARP) of the transmitted signal increases. To prevent distortion in high PAPR signal, power amplifier (PA) should work at larger power back-offs and consequently lower efficiencies [1]. During the last decade, many efficiency enhancement techniques like Doherty amplifier [2,3], envelope tracking (ET) [4] and linear amplification with nonlinear component (LINC) [5] have been proposed to solve this problem.

An architecture that can be used to increase the efficiency, while maintaining high linearity, is a delta sigma modulator (DSM)-transmitter [6–10]. DSM-transmitter converts envelope varying signal to a constant envelope signal with a zero PAPR using 1-bit DSM. Therefore, the PA can work without power back-off and in its most efficient regions. Because of the constant envelope signal, a high efficiency switched mode PA (SMPA) with theoretically 100% efficiency can be also used with this structure [11]. DSM presents high linearity performance because it moves most of the quantization power to the out of band region. Also, DSMs are very reconfigurable, so, they have a potential to be used for multi-band multi-standard software define radio (SDR) applications [6,9,12].

The major drawback of DSM-transmitters is high clock speed requirement [9]. In DSM-transmitters, the clock speed of the DSM should be much higher than the bandwidth of the signal in order to have good signal to noise and distortion ratio (SNDR). In other words, the linearity performance of the DSM-transmitter is dependent on the oversampling ratio (OSR) of the DSM and it can limit the input signal bandwidth.

In this paper, a low complexity time-interleaved parallel DSM is used in DSM-transmitter architecture to decrease clock speed requirement for achieving specific signal quality. So, transmitter can be used for larger input signal bandwidths without the need of high clock speed. A signal processing technique based on feedforward and feedback matrices is used to design this time-interleaved parallel DSM. By using this time-interleaved parallel DSM with four parallel branches the bandwidth of the DSM-transmitter can improve four times without the need of increasing clock speed. Therefore, combining this two-level low complexity time-interleaved parallel DSM and switch mode PA, can be resulted high power efficiency, bandwidth and linearity for DSM-transmitter without the need of very high design area. This is very important issue in today's wireless communication systems which are using highly varying envelope signal with complex modulated

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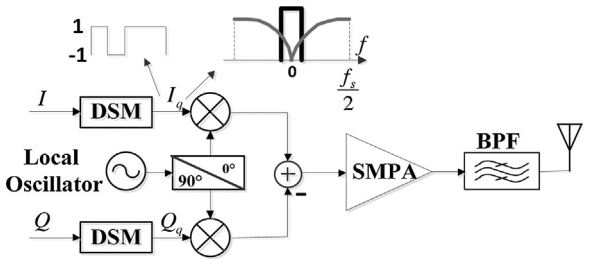


**Fig. 1.** Block diagram of the DSM-transmitter.

technique, such as orthogonal frequency division multiplexing (OFDM) modulation.

The paper is organized as follows. In Section 2, the architecture of DSM-transmitter is described. In Section 3, the low complexity time-interleaved parallel DSM is expressed and simulation results for this architecture are provided. In Section 4, the low complexity time-interleaved parallel DSM is used in DSM-transmitter in order to enhance the bandwidth of the transmitter. Finally, the Section 5 concludes the paper.

## 2. DSM-transmitter

The block diagram of the DSM-transmitter is shown in Fig. 1. It consists of four main sections: first, a DSM to convert the baseband signal into quantized two-level signal by using one-bit quantizer, Second, a frequency up-converter, third, an SMPA and last, band-pass filter to remove the quantization noise. In DSM-transmitter, the quadrature components, $I$ and $Q$, of input signal are quantized separately to the two discrete levels, −1 and 1, so the envelope and phase of the quantized signal before up conversion can be written as [13]:

$$\left|S_q\right| = \sqrt{I_q^2 + Q_q^2} = \sqrt{2} \tag{1}$$

and

$$\angle S_q = \tan^{-1}\left(\frac{I_q}{Q_q}\right) = \frac{\pi}{4}, \frac{3\pi}{4}, \frac{5\pi}{4}, \frac{7\pi}{4} \tag{2}$$

where, $I_q$ and $Q_q$ are quantized quadrature components and $S_q$ is the quantized signal in DSM-transmitter before up conversion. This constant envelope signal is ideal to obtain the highest efficiency from SMPAs.

## 3. Time-interleaved parallel DSM

To reduce the high-sampling frequency and clock speed requirements of the delta sigma modulators many Parallel processing techniques have emerged.

In one approach, the Hadmard transform is used to decompose the input spectrum into several sub-bands [14,15], which are then applied to separated DSMs. In this case each sub-band needs lower clock speed for modulation. After modulation, the Hadmard transformer is applied again to recombine the outputs of DSMs, and the modulated form of the input signal is reconstructed at the output.

A parallel DSM architecture is proposed by combining multiple DSMs in parallel, along with analog pre-processing of input signal and digital post processing of the output signals [16].

In another approach, a filter bank is used to break the signal to the smaller bandwidths signals. So, the modulator clock speed requirement for each of these sub-bands is reduced considerably [17]. This technique is usually called frequency band decomposition.

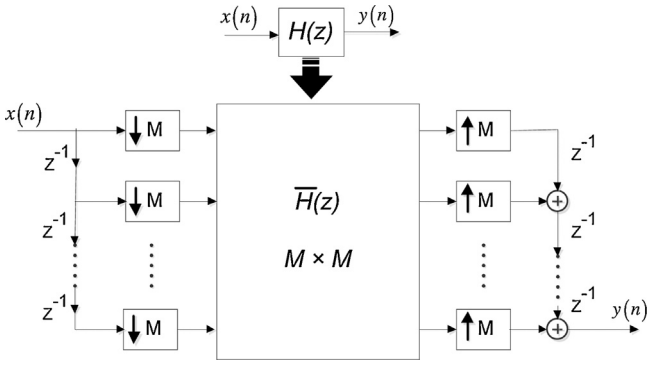


**Fig. 2.** Equivalent circuit for discrete system transfer function, *H(z)*.

In an another research, the processing speed of the modulator was reduced $M$ times by using $M$ interconnected modulators working in parallel with each other while running at the same clock speed [9,18–20]. This technique is called time-interleaved delta sigma approach. In present study, this technique is used to enhance the supported bandwidth without the need of increasing the clock speed.

### 3.1. Low complexity parallel time-interleaved DSM

Assuming that $H(z)$ is an arbitrary discrete system transfer function with single-input and single-output, an equivalent circuit for $H(z)$ can be achieved by applying polyphase multi-rate technique as shown in Fig. 2 [18].

The $\tilde{H}(z)$ in Fig. 2 is a $M \times M$ transfer function and is given by [9,18–20]:

$$\tilde{H}(z) = \begin{bmatrix} E_0(z) & E_1(z) & E_2(z) & \cdots & E_{M-1}(z) \\ Z^{-1}E_{M-1}(z) & E_0(z) & E_1(z) & \cdots & E_{M-2}(z) \\ Z^{-1}E_{M-2}(z) & Z^{-1}E_{M-1}(z) & E_0(z) & \cdots & E_{M-3}(z) \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ Z^{-1}E_1(z) & Z^{-1}E_2(z) & Z^{-1}E_3(z) & \cdots & E_0(z) \end{bmatrix} \tag{3}$$

where, $E_j(z)$ is the polyphase component of $H(z)$. If $h(n)$ and $e_j(n)$ are the time domain presentations of $H(z)$ and $E_j(z)$, the relation between $H(z)$ and $E_j(z)$ is as follows:

$$e_j(n) = h(Mn + j) \quad 0 \le j \le M - 1 \tag{4}$$

and

$$H(z) = \sum_{j=0}^{M-1} z^{-1} E_j(z^M) \tag{5}$$

The $M$-time down-samplers at the input of $\tilde{H}(z)$ shows that $\tilde{H}(z)$ would work at a clock speed M times lower than its equivalent $H(z)$ while providing the same performance. At the output of $\tilde{H}(z)$, a series of $M$-time up-samplers and delays should be used to construct the output signal.

So, an equivalent circuit for second order delta sigma modulator can be achieved by applying polyphase multi-rate technique to reduce the sampling frequency requirements.

The second order modulator is shown in Fig. 3. By assuming that the quantization noise is uncorrelated to the input signal, the quantizer may be modeled as an adder that introduces a quantization error, $e(n)$, to the signal [13,21,22]. The relation between the output