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A fully integrated 2.4 GHz CMOS high power amplifier using parallel class A&B power amplifier and power-combining transformer for WiMAX application

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ABSTRACT

A new structure integrated power amplifier with watt-level output power is presented in a standard 0.18 μm CMOS process for WiMAX applications. A parallel cascode class A&B power amplifier with optimized widths is proposed to increase linearity and efficiency simultaneously. A novel interleaved PCT power combiner is proposed for increasing output power that combines output current of two similar class A&B power amplifiers. Proposed interleaved transformer heightens coupling factor compared to typical transformer.

The proposed power amplifier with 3.3 V power supply provides maximum output power of 32.5 dBm and power added efficiency of 37.9% at 2.4 GHz operating frequency. The proposed power amplifier exhibits high output power of 32.3 dBm at 1 dB compression point. The simulation results for proposed PA with modulated OFDM signal show that −31 dB error vector magnitude at the average power of 25 dBm can be achieved.

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1. Introduction

Today, fully integration of analog, digital and even RF functions is inevitable work in advanced wireless communication industry in order to reduce manufacturing cost and size. The most effective way for this implementation has been CMOS technology that already is dominant way for implementation of RF, analog and baseband digital transceiver circuits [1]. Power amplifiers are main blocks for constructing wireless communication systems [2]. Also, radio frequency power amplifiers are one of challenging blocks in designing RF transceivers. Because of low cost and easy fabrication of CMOS technology, this technology has been proposed and used for designing and implementation of many power amplifiers at various applications [3–7].

While a PA consumes a majority of DC power in the RF front-end side, a highly efficient PA with high output power is necessary for longer battery life in wireless applications. However, because of low breakdown voltage and lossy substrate of CMOS compared to III–V devices, the design of an efficient CMOS PA with high output power remains a challenging task [8]. In other word, the design of a high performance power amplifier has bound designers to use complicated procedures for compensating mentioned problems of CMOS technology [9]. When CMOS technology is famous for low power driving; additional function is required for increasing output power of PA, i.e. power combiner that combines several power cells in order to achieve high output power. The schematic diagram of power combiner is shown in Fig. 1.

As shown in Fig. 1, *M* differential power amplifiers are connected to the power combiner which combines the output current or voltage of power amplifiers. The combiner also converts the differential signals to single ended signals.

Recently, the most successful attempts for creating a component that performs impedance matching and power combining simultaneously have been done. One of functions that fulfill this work is transformer that according to the class of combining current or voltage is classified into series-combining transformers (SCTs) and parallel-combining transformers (PCTs), respectively [10]. Transformers are superior to transmission-line based parallel-combining structures in terms of integration and design simplicity [11]. They also have wider operating bandwidth and less optimization issues than the LC-based network exploited in [12].

Wireless communications create many challenges upon power amplifiers for current and modern applications. The requirement of high-speed date rate causes using of complex digitally modulated signals at OFDM mode. These days WiMAX standard is one of the prominent standards in the world. WiMAX that stands for “Worldwide Interoperability for Microwave Access” is the last technology and generation for broadband wireless access. It is based on IEEE 802.16 standards [13]. The WiMAX standard provides

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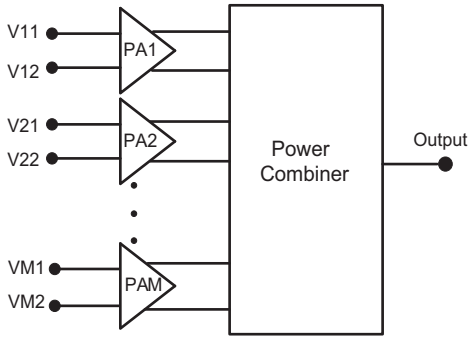

Fig. 1. Block diagram of parallel-combining PA.

up to 15 Mbps of data rate and 28 MHz of signal bandwidth with a wireless coverage of four to six miles [14]. However, using OFDM modulation in WiMAX applies a lot of restrictions in scaled CMOS technology [15]. Dealing with radio frequency (RF) signals modulated with high complexity, PAs must simultaneously achieve high output power, high peak-power efficiency, and good linearity [9].

In this work, a fully integrated power amplifier with high output power using a parallel class A&B for WiMAX applications in a standard 0.18 μm CMOS process is presented. In Section 2, a new interleaved power-combining transformer is proposed that can increase coupling coefficient. In Section 3, the design procedure and all components of power amplifier are described. Finally, the simulation results of the new designed power amplifier and the results compared to several other PAs are presented in Section 4.

2. The new interleaved transformer design as power combiner

Recently, power combiners as a method for increasing output power, impedance matching and converting differential to single-ended signal in power amplifier circuits have been extensively used. Also in the last decade, the power combiner architecture in order to produce high power with low voltage CMOS transistors has been noticed. A distributed active transformer (DAT) is one of methods which is used for generating the output power more than 1 W [16]. However, a large area of chip is allocated to DAT and transistors are laid near the transformer in this structure. Because of circular shape of this transformer and coupling the input signal with the transformer, this structure may cause instability [17]. Using a transformer as PCT and SCT with detailed simulations and analytical expressions were analyzed in [10] and then it has been extensively used in designing power amplifiers with high output power. Using PCT as a power combiner was used in [9,10,18–21] and SCT has been used in [15,22–26] for increasing the output power of power amplifiers. The schematic diagram of a 2 × 1:2 transformer is shown in Fig. 2(a). This transformer is constructed from two primary windings which have magnetic coupling with the secondary winding.

Fig. 2(a) shows the outputs of two power amplifiers which are connected to the primary windings of transformer and because of mutual inductance between primary and secondary windings the output current will be the ratio of input current at primary windings. Fig. 2(b) depicts the physical layout of 2 × 1:2 transformer. In order to achieve an output power more than 1 W, in this design PCT is preferred to SCT because PCT has lower area than SCT. Additionally, in terms of power-combining ratio and transformer efficiency PCT is better than SCT.

The idea of interleaved structure is used for designing the power-combining transformer [27]. The top view of proposed 2 × 1:2 interleaved transformer is shown in Fig. 2(c). Each wide metal in Fig. 2(b) by using the interleaved structure is divided into two metals with equal widths for increasing the coupling coefficient, and are placed in parallel between secondary adjacent layers. The three-dimensional proposed interleaved power-combining transformer layout is shown in Fig. 2(d). To study more over this layout, each first winding of proposed transformer is shown with one secondary winding in Fig. 2(e). In Fig. 2(e), if two primary windings laying over together with the secondary winding, this layout of transformer will be the same layout in Fig. 2(c). For the stability purpose, the input ports align in the left side and the output port is aligned in the right side of the transformer. The proposed transformer has two input ports ($P1$, $P2$) and one output port ($P3$). The input ports ($P1$, $P2$) are connected to the drain of power amplifier and the output port ($P3$) is connected to the resistive load. The standard 0.18 μm CMOS process with six aluminum metal layers was used for designing this transformer.

Four metal layers are used in this transformer which the main metals are located in the top layer. The underpass layers are placed in the bottom metal layers that have 0.53 μm thickness. The proposed interleaved transformer has a size of 780 μm × 800 μm. The thickness of substrate is 200 μm and the metal is Al with conductivity 3.65e7 S/m. In the design procedure of the transformer, the physical parameters such as the outer dimension, metal widths and the spacing between metals are important parameters for optimizing the transformer. The outer dimension effectively determine self-inductance values for mutual coupling, the widths and thickness determine the quality factors for primary and secondary winding inductors and the spacing between two adjacent metals is trade-off between capacitive coupling and mutual coupling in transformers. At first, because the output power more than 1 W is required for designing the power amplifier, metal widths in this transformer and the spacing of metals are chosen 30 μm and 5 μm, respectively. After using the method of interleaving, the metal widths are chosen 15 μm.

In this paper, two transformers are designed and simulated using ADS momentum; the interleaved and typical transformer and their results are compared at 2.4 GHz frequency in Table 1. All specifications of two transformers such as area, spacing, technology, and metal thicknesses are equal and the only difference between them is the interleaved metals.

The inductance values of primary and secondary windings from the layout are calculated as follows:

$$L_1 = \frac{I_m(Z_{11})}{\omega} \tag{1}$$

$$L_2 = \frac{I_m(Z_{22})}{\omega} \tag{2}$$

where L_1 and L_2 are primary and secondary inductances of the transformer. As shown in Table 1, the interleaved structure causes the self-inductance of the primary and secondary windings to decrease. The self-inductance of the primary and secondary windings of typical transformer is 1.9 nH and 4.79 nH, respectively and these values for the interleaved transformer are 1.58 nH and 4.13 nH. Also, the quality factor Q, the coupling coefficient K, and the mutual inductance M are calculated as follows:

$$Q_P = \frac{I_m(Z_{11})}{R_e(Z_{11})}, \qquad Q_S = \frac{I_m(Z_{22})}{R_e(Z_{22})} \tag{3}$$

$$K(L_1, L_2) = \frac{M}{\sqrt{L_1 L_2}} = \sqrt{\frac{(Y_{11}^{-1} - Z_{11})Z_{22}}{I_m(Z_{11})I_m(Z_{22})}} \tag{4}$$

where Q_P and Q_S are the quality factor for primary and secondary winding, respectively. The quality factor for primary and secondary windings of the typical transformer is 10.32 and 16.52, respectively. Because of reducing the self-inductance in the interleaved structure, the quality factor for the proposed transformer decreases to

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