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LETTER

# A current-mode analog multiplier/divider based on CCCDTA

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**Abstract**

A novel simple current-mode analog multiplier/divider, based on current-controlled current-differencing transconductance amplifier (CCCDTA), is presented. The proposed circuit employs only single CCCDTA without any external passive element requirement and it can work as multiplier and divider without changing its topology. In addition, the proposed circuit can work as gain-controllable current amplifier. The circuit performances are depicted through PSPICE simulations. The simulated results show that: for $\pm 1.5$ V power supply, the total harmonic distortion is about 0.1%, the $-3$ dB bandwidth is more than 26.94 MHz, maximum input range is about $100\,\mu A$ and the output current is low sensitive to temperature variations.


***Keywords:*** Analog; CCCDTA; Current mode; Divider; Multiplier

## 1. Introduction

Analog multiplier and divider are important building blocks in continuous-time signal processing. They can be found in many tasks: for instance, modulation, measurement, instrumentation, and control systems [1–3]. Many techniques to implement multiplier and divider have been presented as follows. The multiplier and divider based on translinear property of a bipolar junction transistor (BJT) [4], based on square-law characteristic of a CMOS [5], using switched capacitor (SC) [6]. Unfortunately, all techniques are suitable for working in voltage mode. They cannot be applied to employ in a current-mode signal-processing circuit, which are continually more popular in present due to several features such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry, and lower power consumption [7,8].

Realizations of the current-mode multipliers and dividers can be separated into two main techniques, which are continuous-time signal and sampled-time signal based on switched-capacitor or switched-current technique [9,10]. The latter method needs to inevitably employ clock signal to activate the circuit. Consequently, the problems are clock feed through, narrow bandwidth of output signal, and aliasing. In addition, it requires a precise clock-signal generated from a high-performance clock generator, thus it occupies a large area in monolithic chip. For continuous-time multipliers/dividers, the most techniques use square law of MOS device [3,11,12]. They confront several drawbacks, for instance, requiring matched elements of MOS devices, performing narrow frequency response, providing low dynamic range, depending on ambient temperature, and encountering high total harmonic distortion. Although, in the past, circuit techniques that employ OTAs to implement analog multiplier and divider have been proposed [13]. However, they function in voltage mode. Additionally, only multiplication functions are realized and the circuit bandwidths are only 2 MHz.

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This work is organized to propose novel current-mode analog multiplier/divider using current-controlled current-differencing transconductance amplifiers (CCCDTA) as the active building block recently proposed in [14]. The features of proposed circuit are that: the proposed multiplier/divider can multiply and divide two current signals throughout two quadrants with a wide range of frequencies, without changing its topology, the circuit is insensitive to temperature, low harmonic distortion, low-power consumption and output current can be controlled via input bias current. Furthermore, not only working as a current multiplier/divider, the proposed circuit can function as a gain-controllable current amplifier. The performances of proposed circuit are illustrated by PSPICE simulation, they show good agreement as depicted.

## 2. Principle of operation

### 2.1. Basic concept of CCCDTA

Since the proposed circuit is based on CCCDTA, a brief review of CCCDTA is given in this section. Basically, the CCCDTA is composed of translinear elements, mixed loops, and complementary current mirrors. Generally, its properties are similar to the conventional CDTA, except that input voltages of CCCDTA are not zero and the CCCDTA has finite input resistances $R_p$ and $R_n$ at the $p$ and $n$ input terminals, respectively. These intrinsic resistances are equal and can be controlled by the bias current ($I_B$) as shown in the following equation:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix}. \quad (1)$$

When

$$R_p = R_n = \frac{V_T}{2I_B} \quad (2)$$

and

$$g_m = \frac{I_C}{2V_T}, \quad (3)$$

where $g_m$ is the transconductance gain of the CCCDTA and $V_T$ is the thermal voltage. The symbol and the equivalent circuit of the CCCDTA are illustrated in Fig. 1(a) and (b), respectively.

### 2.2. Proposed current-mode analog multiplier/divider

The proposed multiplier/divider based on CCCDTA is shown in Fig. 2. It employs only single CCCDTA. From routine analysis and using the CCCDTA properties, we will get output current as

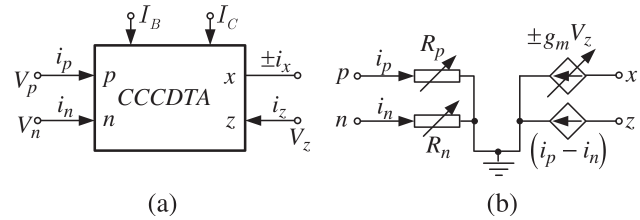


**Fig. 1.** CCCDTA: (a) symbol and (b) equivalent circuit.

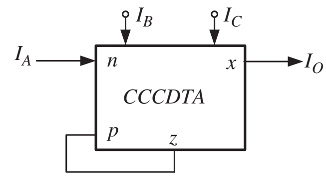


**Fig. 2.** Proposed current-mode multiplier/divider.

$$I_O = \frac{I_A I_C}{8I_B}. \quad (4)$$

From Eq. (4), it is clearly seen that $I_O$ is a result of either, multiplying of $I_A$ and $I_C$, or dividing of $I_A$ and $I_B$. Due to being a positive value of $I_B$ and $I_C$, the proposed circuit can be a 2 quadrant multiplier/divider. In addition, if $I_A$ is input current, the proposed circuit can work as current amplifier, which the magnitude of output current can be controlled by $I_B$ or $I_C$. Furthermore, the circuit is theoretically temperature insensitive owing to no term of $V_T$.

### 2.3. Non-ideal case

In practice, the CCCDTA is possible to work with non-ideality. Its properties will change to

$$I_z = \alpha_p I_p - \alpha_n I_n + \varepsilon_z \quad (5)$$

and

$$I_X = \beta g_{m22} V_z + \varepsilon_x, \quad (6)$$

where $\alpha_p$, $\alpha_n$, and $\beta$ are transferred error values deviated from one. While $\varepsilon_z$ and $\varepsilon_x$ are the offset currents at $z$ and $x$ terminals, respectively. By straightforward analysis of the internal construction of CCCDTA in Fig. 3, we will obtain the $\alpha_p$, $\alpha_n$ and $\varepsilon_z$ as

$$\alpha_p = \frac{g_{m6} g_{m12} g_{m19} + g_{m3} g_{m13} g_{m18}}{g_{m12} g_{m18} (g_{m6} + g_{m3} + g_{\pi 3} + g_{\pi 6})}, \quad (7)$$

$$\alpha_n = \frac{K_4 + K_5}{g_{m5} + g_{m2} + g_{\pi 2} + g_{\pi 5}}, \quad (8)$$

$$\varepsilon_z = I_B \begin{bmatrix} K_1(g_{m6} - g_{m3}) + (g_{m20} - g_{m21}) K_2 \\ +K_3(g_{m2} - g_{m5}) + K_4 - K_6 - K_5 + K_7 \end{bmatrix}, \quad (9)$$