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A new burst-mode clock recovery technique for optical passive networks

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Abstract

A new burst-mode clock recovery device regenerating the clock at the timing of the first data bit from the input burst-mode packet has been proposed and experimentally demonstrated. The setup of proposed device is composed of simple logic gates and performs successfully regardless of the unstable delay time of feedback loop in the CDR (clock and data recovery) device. After performance evaluation, we have found that the device successfully generates the clock at 155.52 Mb/s and is able to perform clock recovery with a dynamic range of 21 dB at BER $= 10^{-10}$.
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Keywords: Burst-mode optical transceiver; Clock recovery; Passive optical networks (PON); FTTH (fiber-to-the-home)

1. Introduction

Passive optical networks (PON) for an FTTH (fiber-to-the-home) have been actively researched where a burst-mode transceiver is one of the key modules to realize high-speed digital subscriber line [1–5]. A PON system is a point-to-multipoint optical network where the up-stream data received at an OLT (optical line termination) have the different amplitudes and phases because the distance between the OLT and the ONUs (optical network units) are different. Hence, a fast and stable clock recovery from the received packet is the most difficult problem [2–5]. Recently, the all-optical burst-mode clock extraction has been introduced [6]. But, this technique is not suitable for an optical subscriber line, because of the cost and its data format limited to RZ (return-to-zero). A clock recovery techniques using semiconductor devices [7,8] are also presented, where the incoming optical signal is converted to the electrical signal, then the clock phase recovery and burst synchronization are performed. In [7], the fast logic gates and a monostable multivibrator with a feedback loop are used in the clock generator. In [8], a feed forward circuit which extracts the correlated clock among the number of clocks with different phase from ONUs. But, the technique in [8] is more complicated to implement than the technique in [7].

In this paper, we introduce a new technique of burst-mode clock recovery based on [7], where the clock generation principle is described and compared with the conventional techniques. The proposed device is implemented with only simple logic gates and delay lines, and can perform the clock generation for the high-speed burst mode and the continuous mode as well.

2. The PON

As shown in Fig. 1, a typical PON system is a point-to-multipoint, FTTH network where an OLT at the central office is connected to N ONUs at the end users through an

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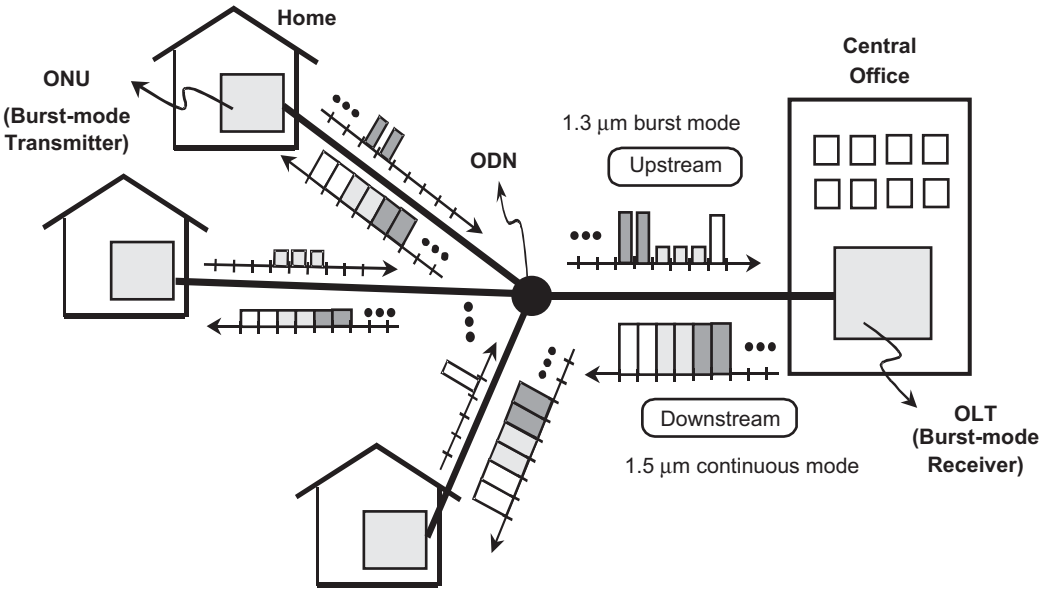

Fig. 1. Structure of a passive optical network.

ODN (optical distribution network). An OLT broadcasts the downstream optical signal in TDM (time division multiplexing) continuous mode to ONUs, and receives the upstream optical signal in TDMA (time division multiple access) burst mode to provide time slot assignments for each ONU. However, the amplitudes and phases of the burst-mode optical packets received by OLT are different because the distance between the OLT and ONUs are not identical. Hence, a fast and stable clock recovery from the received packet is the most important technology to enable the PON system.

In order to compensate the amplitude and phase variation of the burst-mode optical packets from the different ONUs, the burst-mode clock recovery device in [7] has been introduced as shown in Fig. 2. Fig. 2(a) shows the clock generator composed of an XOR gate, two delay lines, an OR gate, and a monostable multivibrator and its timing diagrams of the clock generator are shown in Fig. 2(b). Let one period of the random input signal, e1, be T. The output signal of XOR gate, e3, has level '1' during $< T/2$. The inputs of an OR gate are e3 and e4, and the output signal of an OR gate becomes e5 which is fed back through a monostable multivibrator and delayed for T. A monostable multivibrator detects the rising edge of the e5 signal, and generates the clock signal e6 with level '1' for $T/2$ and level '0' for the other $T/2$. If a delay time in the feedback loop is slightly less than T due to the temperature variation, the clock generator cannot perform the clock recovery as shown in Fig. 3.

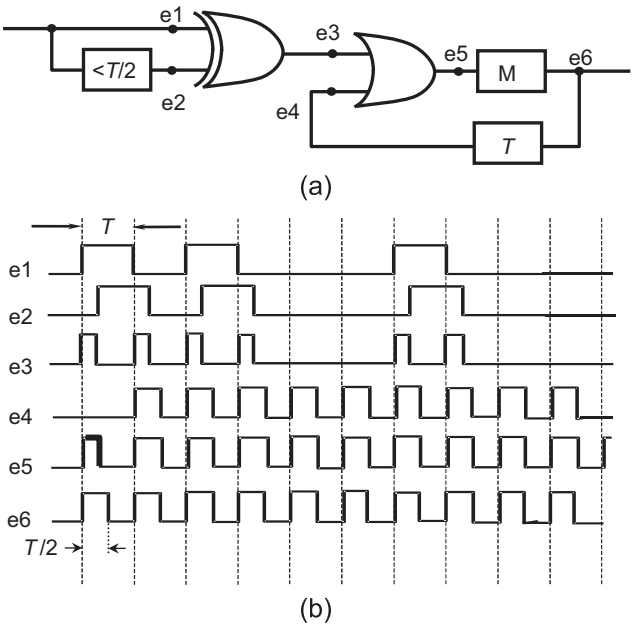

Fig. 2. (a) The burst-mode clock recovery device of US Patent no. US04604756 using a monostable multivibrator with a $T/2$ delay feedback loop and (b) its timing diagram with a monostable multivibrator, M, and a delay line, T.

In Fig. 3(a), if the delay, T_f, in the feedback loop is $T+\varepsilon$ where $\varepsilon > 0$, the output clock is stable because the e6 signal is generated at the rising edge of e3 signal. In other words, the rising edge of e5 signal in Fig. 2(b) depends on the e3 signal and the monostable multivibrator always generates the pulse at the rising edge of e3 signal. Hence, the output clock signal e6 is normally generated. On the other hand, as shown in Fig. 3(b), if the delay, T_f, in the feedback loop is $T-\varepsilon$, the monostable multivibrator is triggered at the rising edge of e4 signal. If this signal is fed back again, the output clock with the rising edge at $T-2\varepsilon$ is generated. When the feedback operation repeats, eventually, the output signal, e6, becomes the DC signal with level '1'. Hence the clock generator will be completely disabled.

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