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Self-controlled 4-transistor low-power min–max current selector

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ABSTRACT

Four cross-coupled MOS transistors operating as switches implement a very compact, fast, low-power and precise minimum and maximum current selector. Local positive feedback allows the circuit to work without the need of any control inputs and ensures very high sensitivity. Experimental results confirm the simulations and the analyzed second-order effects. Applications include min–max current selection and precision differential rectification. An application example of the cell to build a similarity circuit is reported.

1. Introduction

Minimum and maximum (min–max) analog VLSI current selectors are versatile building blocks used in several applications such as nonlinear function synthesis (e.g. fuzzy logic and artificial neural models), neuromorphic systems and full-wave precision rectification.

Current-mode min–max functions can be obtained from winner-take-all (WTA) circuits [1–4]. In particular, the initial proposal in [1], due to its simplicity and scalability, has been the starting point for many min–max circuits in fuzzy logic implementations, such as [5,6] and subsequent modifications [7,8].

Other min–max circuits [9–12] and rectifiers [13–18] with complex topologies allow to implement two-input min–max current selection but the area overhead of those proposals would be high for a compact and simple integration, especially in applications that require a massively parallel implementation of this function, such as image focal-plane image processing and other neuromorphic parallel processing systems.

In this paper, a very compact circuit based on four cross-coupled MOS transistors that by construction do not require external control elements is introduced. The circuit accurately selects the minimum and maximum of two input currents. Because of its simplicity, the proposed circuit outperforms other existing two-input current-selection topologies reported up to now. In the next section, the current switch is introduced and analyzed. The circuit design and simulations are discussed in Section 3 and the circuit second-order behavior is analyzed in Section 4. Experimental results of the measured cell are disclosed in Section 5, while in Section 6 the current selector circuit is applied to perform a selective similarity function to finally conclude in Section 7.

2. The basic circuit

The circuit principle is shown in Fig. 1a. Two cross-coupled switch pairs detect at any time the minimum and the maximum of two input currents, I_1 and I_2, directing them to I_{MIN} and I_{MAX} output lines, respectively.

The proposed circuit is shown in Fig. 1b. It simply consists of the four switch transistors whose gates are connected to the input nodes. Thus, the switches are self-controlled by detecting voltage at their inputs, without any extra circuitry required. All transistor sizes are identical.

For the analysis, the circuit can be interpreted as composed of two current mirrors with cross-coupled input and output nodes. Mirror $M_{1A} - M_{2B}$, controlled by V_1, implements the parallel switches and mirror $M_{2A} - M_{1B}$, controlled by V_2, the crossed ones.

2.1. Ideal analysis

For the sake of simplicity, let us set the output voltage $V_{REF} = 0\,V$. Thus, nodes V_1 and V_2 completely determine the transistors' operating conditions. Assuming saturated transistors, with no Early (or channel-length modulation) effect and ideal current mirroring, and applying the Kirchhoff current law, the only compatible solution for the circuit is

$$I_1 = I_{D1A} + I_{D1B} = I_{D1A} + I_{D2A} \tag{1a}$$

$$I_2 = I_{D2A} + I_{D2B} = I_{D2A} + I_{D1A} = I_1 \tag{1b}$$

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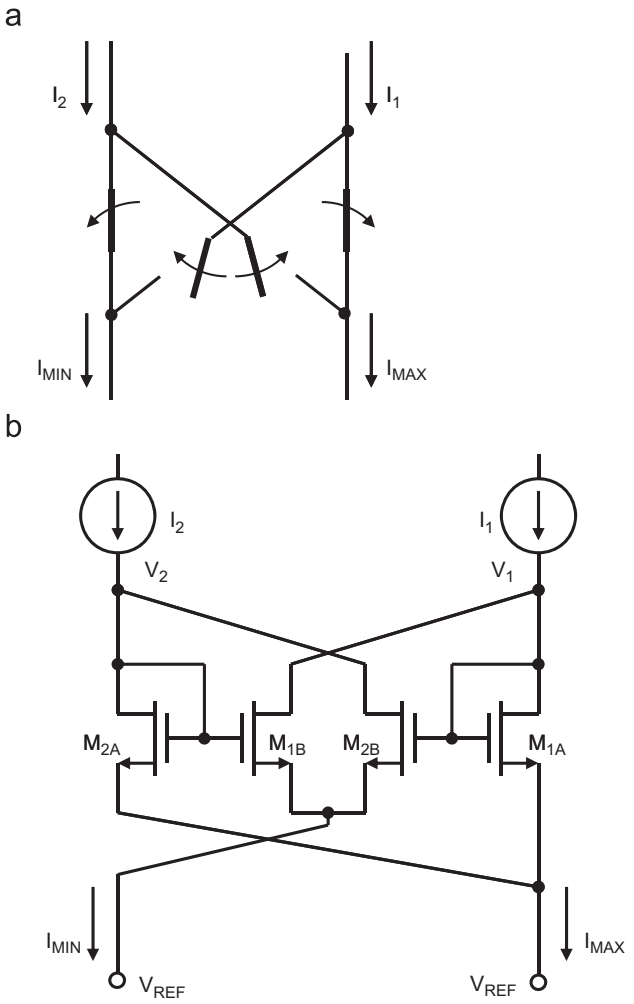

Fig. 1. (a) Circuit principle and (b) NMOS min–max current switch.

Thus, input currents have to be necessarily identical ($I_1 = I_2 = I_0$, where I_0 is an arbitrary input current) to accomplish the equation constraints under those ideal conditions. At this equilibrium point, all transistors operate under the same electrical conditions and, because of circuit symmetry, $I_{D1A} = I_{D1B} = I_{D2A} = I_{D2B} = I_0/2$. Also, since $V_1 = V_2$ and $V_{GS} = V_{DS}$ for all transistors, they all operate in the saturation region, validating the previous assumption. Finally, $I_{MAX} = I_{MIN} = I_0$. This implies that the circuit will only operate with all transistors saturated if $I_1 = I_2$.

Starting from the equilibrium point, let us assume that one of the inputs slightly increases, e.g., $I_1 = I_0 + \Delta I$. This rises V_1, because M_{1A} has to drain now $I_0/2 + \Delta I$. Thus, M_{2B} will in turn drain $I_0/2 + \Delta I$. This leaves M_{2A} draining less current, $I_0/2 - \Delta I$, reducing V_2 and the current drained by M_{1B} also down to $I_0/2 - \Delta I$. This produces a new increase in the M_{1A} current to $I_0/2 + 2\Delta I$, and this positive-feedback loop will continue until mirror transistors $M_{1A} - M_{2B}$ drain $I_1 = I_0 + \Delta I$ and $I_2 = I_0$, respectively, while $M_{2A} - M_{1B}$ turn off, regardless of the ΔI value. Notice also that, with no Early effect, M_{2B} has to operate in linear region to drain smaller current than M_{1A}. Conversely, when $I_1 < I_2$, M_{2A} and M_{1B} will drain I_2 and I_1, respectively, while mirror $M_{1A} - M_{2B}$ turns off. Summarizing, in a WTA-like competition, the mirror whose diode-connected transistor receives the largest current will finally drive both input currents and turn off the complementary mirror. In both cases, the larger input current is routed to the I_{MAX} output and the smaller one, to I_{MIN}.

2.2. First-order large-signal analysis

In real devices, a small enough input current difference does not turn off the loser mirror. If the Early effect is taken into account to obtain the circuit DC input–output characteristic around the equilibrium point, a first-order small-signal analysis leads to the same condition as Eq. (1), i.e., any ΔI produces the loser mirror to turn off, because the MOS output resistance r_0 in this model is constant. Thus, large-signal equations have to be used for this analysis to obtain a more realistic result.

When applying opposite differential currents with I_0 common-mode input current as shown in (2), V_1 and V_2 suffer an opposite variation until the Early effect compensates for the ΔI current difference

$$I_1 = I_0 + \frac{\Delta I}{2} = I_{D1A} + I_{D1B} \tag{2a}$$

$$I_1 = I_0 - \frac{\Delta I}{2} = I_{D2A} + I_{D2B} \tag{2b}$$

Considering the first-order MOS drain current model

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^{\alpha}(1 + \lambda V_{DS}) = I_Q(1 + \lambda V_{DS}) \tag{3}$$

where β is the large-signal transconductance parameter, α is the current-law exponent of the strong inversion MOS transistor ($\alpha = 2$ for the long-channel model), and λ is the Early effect parameter.

Substituting (3) into (2), and assuming reduced Early effect and small ΔI, the following approximate V–I relation between the differential input current and the input voltage is obtained

$$\Delta I = I_1 - I_2 = \lambda(V_1 - V_2)(I_{Q1} + I_{Q2}) \cong \lambda I_0(V_1 - V_2) = \frac{2}{r_0}\Delta V \tag{4}$$

where r_0 stands for the transistor output resistance with $I_0/2$ biasing. I_{MAX} and I_{MIN} are obtained as

$$I_{MAX} = I_{D1A} + I_{D2A} = \frac{\beta}{2}[(V_1 - V_T)^{\alpha}(1 + \lambda V_1) + (V_2 - V_T)^{\alpha}(1 + \lambda V_2)] \tag{5a}$$

$$I_{MIN} = I_{D1B} + I_{D2B} = \frac{\beta}{2}[(V_2 - V_T)^{\alpha}(1 + \lambda V_1) + (V_1 - V_T)^{\alpha}(1 + \lambda V_2)] \tag{5b}$$

Subtracting expressions (5), and assuming small input voltage variations,

$$I_{MAX} - I_{MIN} \cong \lambda g_m \Delta V^2 \tag{6}$$

where g_m is the transistor transconductance for $I_0/2$ biasing. Substituting (4) into (6), the differential output current is obtained as a function of the differential input current,

$$I_{MAX} - I_{MIN} \cong \frac{g_m r_0}{2}\frac{\Delta I^2}{I_0} = \frac{A_0}{2}\frac{\Delta I^2}{I_0} \tag{7}$$

where $A_0 = g_m r_0$ is the transistor intrinsic gain. Since $I_{MAX} - I_{MIN}$ is parabolic around the equilibrium point, because of symmetry considerations, I_{MAX} and I_{MIN} will also be parabolic around it. The first derivative of a parabolic expression is only 0 at its minimum. This result confirms that the circuit performs with the continuous derivative of a real system a good approximation of the desired peak shape.