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Low-voltage low-power bulk-driven analog median filter

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ABSTRACT

This paper presents low-voltage (LV) low-power (LP) voltage-mode analog median filter based on winner-take-all (WTA) and loser-take-all (LTA) circuits. The LTA and WTA CMOS structures are performed utilizing bulk-driven (BD) MOS transistor (MOST) technique, enabling circuits to operate under low supply voltage of only ±0.25 V and consume extremely low-power in micro range. In addition to the simple topology of the proposed circuits, they provide high accuracy. Moreover, the common mode voltage range is near rail-to-rail. Eventually, to verify the functionality of the proposed circuits, the simulation results are carried out in Cadence environment using triple-well 0.18 μm CMOS process.

1. Introduction

Min "loser-take-all" (LTA), Max "winner-take-all" (WTA) and median are crucial rank order filters [1], which have various powerful applications in nonlinear signal processing systems. WTA and LTA are paramount nonlinear building blocks, which have been employed extensively in various signal processing applications such as: realizing fuzzy controllers [2], neural networks [3], precision rectifiers [4] and many others. Median filter has emerged as one of the most attractive nonlinear rank order filters, which is useful for noise suppression. The median filtering algorithm was firstly suggested by Tukey [5,6] for nonlinear smoothing of data and various studies have been introduced in literature about this concept [7–11]. Median filter can effectively suppress the impulsive noise, while perfectly preserve edge information. However, the edge information represents the essential features in images and determines the image quality. Therefore, median filters are very useful in image processing applications [12,13]. Moreover, median filters have been effectively used for speech smoothing and biomedical signal processing [11,14–16].

The increasing need for battery powered electronic devices imposes tight constraints on circuit designers. Since such devices have to be smaller in size and should operate perfectly for longer time without recharging or changing the battery. Thus LV LP circuits become essential for battery powered devices fabrication. Powerful CMOS techniques have emerged for realizing high performance LV LP analog circuits. Among them the nonconventional techniques, i.e. bulk driven (BD), floating gate (FG), quasi floating gate (QFG), bulk-driven floating-gate (BD-FG) and bulk-driven quasi-floating-gate (BD-QFG) MOS transistor [17,18].

In this work BD technique is utilized to realize simple CMOS structures of LV LP LTA and WTA circuits. However, unlike the conventional voltage-mode LTA/WTA the proposed CMOS structure of the LTA/WTA offers a current output terminal, which increases their versatility. For instance, numerous applications include: digital-to-analog converter, chopper modulator, programmable adder/subtractor, half-wave rectifier and full-wave rectifier have been developed in Ref. [19] using LTA circuit which has current output terminal. Moreover, by a proper arrangement of BD-LTA and BD-WTA circuits LV LP median filter is obtained. Thus the attractive features of these circuits can be exploited effectively in low-voltage analog systems.

This paper is organized as follows: Section 2 presents the internal structures of the LV LP LTA and WTA based on BD technique. Section 3 shows the proposed LV LP median filter. Section 4 shows the simulation results, and Section 5 is the conclusion.

2. Low-voltage low-power BD-LTA/WTA

2.1. BD-LTA/WTA circuit description

The symbol of the proposed BD-LTA/WTA circuit is presented in Fig. 1(a). It has two voltage inputs (y_1, y_2), one voltage output

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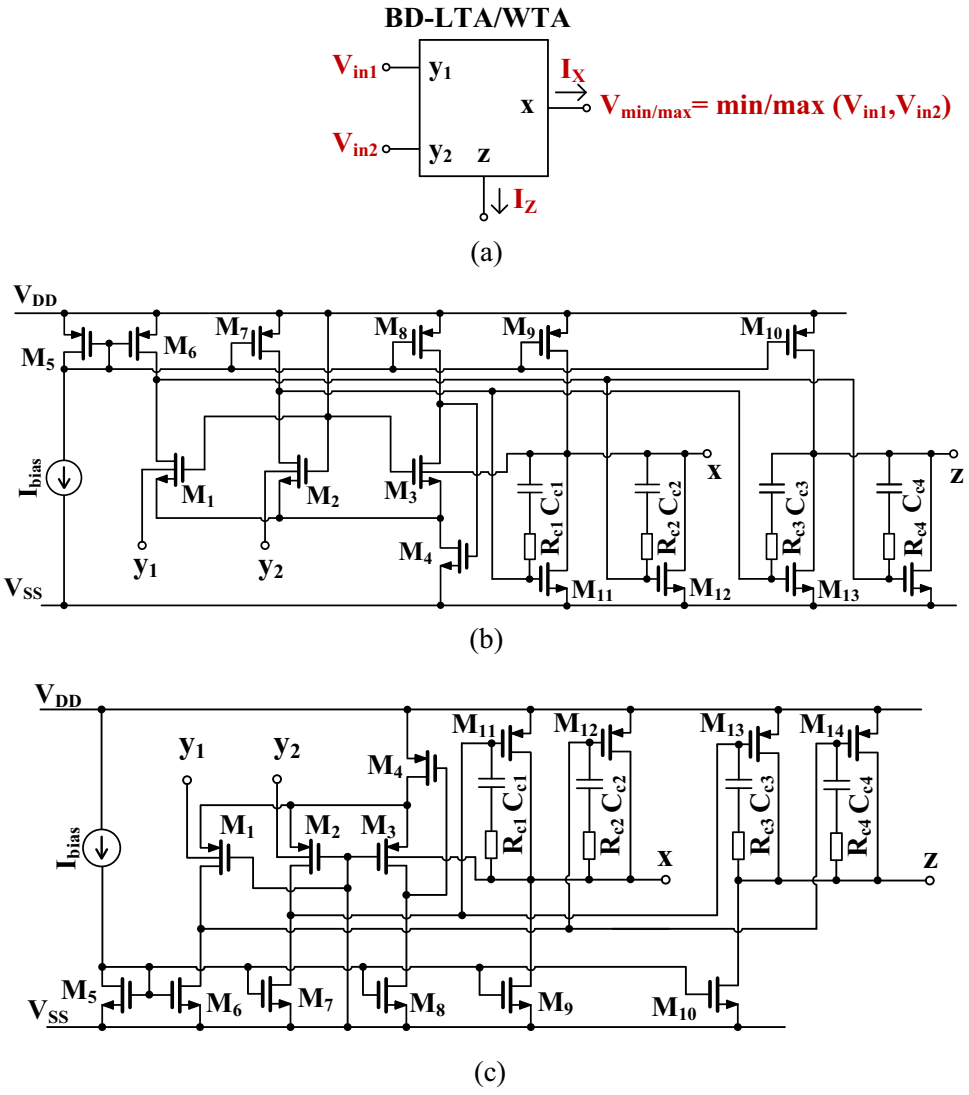

Fig. 1. (a) Symbol BD-LTA/WTA, (b) proposed CMOS structure of BD-LTA, (c) proposed CMOS structure of BD-WTA.

(x) and one current output (z). The output voltage that appears on the x terminal is equal to the minimum/maximum value of the input voltages V_{in1} and V_{in2} that applied to the terminals y_1 and y_2, respectively, i.e. $V_{min/max}$ = min/max (V_{in1}, V_{in2}). The currents output of z and x terminal are equal, i.e. $I_z = I_x$.

The proposed BD-LTA/WTA is obtained by merging the structures of two voltage followers based on op-amp in one effective structure. Consequently, the number of transistors and the power consumption of the BD-LTA/WTA are decreased. The CMOS structure of the BD-LTA and BD-WTA are shown in Fig. 1(b) and (c), respectively. The structure contains two identical two stage op-amps with negative feedback as a voltage follower. However, op-amps with NMOS differential pair have implemented to realize the LTA circuit, while op-amps with PMOS differential pair are used in WTA case. The first op-amp is created by M_1, M_3, M_4, M_6, M_8 as first stage and M_9, M_{12} as second stage. The second op-amp is created by M_2, M_3, M_4, M_7, M_8 as first stage and M_9, M_{11} as second stage. The advantage of this topology is that transistors M_3, M_4, M_8, and M_9 are common for both op-amps. Also note that due to the high transconductance gain of the two stage op-amp, the BD-LTA and BD-WTA circuits are able to distinguish small input differences.

The function of each transistor is as follow: the bulk-driven transistors M_1, M_2, M_3 create the inputs and transistors M_6, M_7, M_8 create the active loads for the first stages. Transistor M_4 creates a tail current source for both first stages and is based on flipped voltage follower principle [20]. Transistors M_{11}, M_{12} create the second stages with common active load created by transistor M_9. Transistors M_{10}, M_{13}, M_{14} are used to create identical current copy of x to z terminal. Transistor M_5 and I_{bias} are used to set the bias current for the circuit. The compensation networks R_{c1}–R_{c4} and C_{c1}–C_{c4} are used to assure circuit stability. The negative feedback is created by connecting the output of the second stage x to the input bulk terminal of transistor M_3, hence the voltage transfer between the y_1, y_2 and x is assured.

The principle of operation of the BD-LTA in Fig. 1(b) is as follows: if $V_{in1} > V_{in2}$ then the drain voltage of M_1 is much lower than the drain voltage of M_2 and the gate voltage of M_{11} is much higher than the gate voltage of M_{12}. Therefore, the drain current of the current source transistor M_9 will flow through transistor M_{11} which in its turn means that only the second op-amp will be active. Consequently, the output voltage V_{min} follows the input voltage V_{in2}. The same principle is valid if $V_{in2} > V_{in1}$ then only first op-amp is active and the output voltage V_{min} follows the input voltage V_{in1}. Hence, the output follows only the minimum input voltages. Likewise, the operation principle of the BD-WTA in Fig. 1(c) can be derived from the operation principle of the BD-LTA. Consequently, the output follows only the maximum input voltages.