Int. J. Electron. Commun. (AEÜ) 70 (2016) 398–408

Contents lists available at ScienceDirect

International Journal of Electronics and Communications (AEÜ)

journal homepage: www.elsevier.com/locate/aeue

An evolutionary approach based design automation of low power CMOS Two-Stage Comparator and Folded Cascode OTA

K.B. Maji [a], R. Kar [a,*], D. Mandal [a], S.P. Ghoshal [b]

[a] Department of Electronics and Communication Engg., NIT, Durgapur, India
[b] Department of Electrical Engg., NIT, Durgapur, India

ARTICLE INFO

Article history:
Received 6 July 2015
Accepted 23 December 2015

Keywords:
Circuit sizing
Two-Stage Comparator
FCOTA
TSC
Simplex-PSO
Analog integrated circuits

ABSTRACT

This paper presents an evolutionary approach to design CMOS Two-Stage Comparator (TSC) and CMOS Folded Cascode Operational Trans-conductance Amplifier (FCOTA) using simplex particle swarm optimization (Simplex-PSO) method. The simplex particle swarm optimization (Simplex-PSO) is a swarm intelligent based evolutionary computation method. Simplex-PSO is the hybridization of Nelder–Mead Simplex method (NMSM) and Particle Swarm Optimization (PSO) without the velocity term. The Simplex-PSO has fast optimizing capability and high computational precision for high-dimensionality functions. This work has focused on the optimization of the area, power and has improved all other performance parameters of the CMOS TSC and CMOS FCOTA with minimum computational time. The proposed Simplex-PSO based circuit optimization technique is relieved from the inherent drawbacks of premature convergence and stagnation, unlike Differential Evolution (DE), Harmony Search (HS). The simulation results prove that Simplex-PSO yields the optimized result with improved functionality. Simulation results obtained for CMOS TSC and CMOS FCOTA prove the effectiveness of the proposed Simplex-PSO method based approach over the reported DE, HS, and PSO in terms of convergence speed, design specifications and design objectives. The optimally designed TSC and FCOTA circuits, individually, occupy the least MOS areas and dissipate the least powers. The simulation plots and results are shown to have the improved performance parameters compared with those of other reported literature. Validation of the design is carried out by Cadence version 5 (IC 5.10.41) of TSMC 0.35 μm technology.

1. Introduction

For last three decades, as the VLSI technology is scaled down, the complexity of the analog integrated circuit (IC) increases drastically. The area occupied by the MOS transistors and power are the most critical issues in the design. Scaling of the MOS transistor improves its size, cost and performance [1]. The designer faces the challenge to reduce the circuit complexity and optimizes the area and power of the circuit. The designer tried some traditional methods to extract the device parameters to minimize area and power, but it is quite lengthy and much time is taken due to non-linearity in the circuit, and does not give the guarantee of optimized parameter extraction [2,3]. PSO is an evolutionary algorithm developed by Eberhart et al. [23,24]. PSO is very simple to implement and its convergence may be controlled by a few number of control parameters. PSO was efficiently utilized in various application areas. Several attempts have been taken towards the identification of benchmark infinite impulse response (IIR) systems with optimal IIR systems derived by PSO [6–8]. Traditionally, analog designs are carried out with analytical methods, and then verified and fine tuned using a SPICE like simulator. Often, it is observed that final design variables (values) are far away from the estimated values obtained from analytical expressions. The difference in predicted design values can be reduced if complex models like BSIM, etc. are used. Then the designer has to seek the help of another simulator, optimizer or programming method to handle those complex equations. Whatever may be the approach, the net time to market increases. The automation of analog design has attracted great attention of the researchers across the world [2]. Analog circuit sizing is a very complex, iterative and tedious process. Classical optimization methods are of two types: deterministic methods and statistical methods. Deterministic techniques like Simplex method [7], Automatic method [8], Goal Programming [9], and Dynamic

* Corresponding author. Tel.: +91 9434788056.
E-mail addresses: kbmaji@gmail.com (K.B. Maji), rajibkarece@gmail.com (R. Kar).

http://dx.doi.org/10.1016/j.aeue.2015.12.019
1434-8411/

Programming [10], etc., are applicable for small size problems. Statistical methods usually start with finding a suitable DC operating point provided by the professional analog designer. After that, a simulation-based tuning method is employed. However, these statistical methods are also time-consuming and do not guarantee the convergence towards the global optimum solution [11]. Hence, classical optimization methods are mostly not suitable for optimal sizing of the total large size analog IC design process.

Heuristic-based approaches are required to solve the large size problems along with several benchmarks [12]. Some mathematical heuristic methods are previously used, e.g., Local Search (LS) [13], Simulated Annealing (SA) [14,15], Tabu Search (TS) [16,17], Scatter Search (SS) [18], Genetic Algorithms (GA) [19,20], etc. However, the efficiency of these methods is mostly dependent on the solution search space, algorithms' control parameters and the number of variables. Most of the heuristic algorithms show the problems of fixing algorithm's control parameters, premature convergence, stagnation and revisiting the same solution over and again. And again, most of the circuit design optimization problems are formulated with different types of variables, constraints and objective functions. Therefore, the aforementioned optimization techniques usually require long computation time when the problem becomes more complicated and involve a very large search space. In order to overcome the drawbacks associated with these optimization methods, a new set of nature inspired meta-heuristic optimization algorithms called swarm intelligence algorithms [21,26,37,48–50] has been proposed. The thought process behind these algorithms is inspired from the collective behaviour of decentralized, self-organized systems. The main objective of this paper is to optimally design the CMOS TSC and CMOS FCOTA with high gain, low power and lesser area compared with those of the methods reported in the existing literature. With particular technology parameters, Simplex-PSO is applied to TSC and FCOTA design problems. The problems considered in this work are the optimal CMOS transistors sizing which would yield the minimum area and power of the total design. The other two parts, i.e., topology selection and actual layout of the circuit are beyond the scope of this study. Simulation based optimization method requires long time to execute and equation based methods are accurate than the former method. Therefore, for analog IC design automation [31,34,35,39,40,47], optimization methods with high accuracy and less execution time are necessary. As a global optimization technique, PSO has smaller number of primitive mathematical operators where in GA, mathematical operations require reproduction, mutation and crossover and hence, it leads to longer computation time and revisiting the same solution over and again. Different from above mentioned studies, this work focuses on optimal sizing of a CMOS Two-Stage Comparator (TSC) and Folded Cascode Operational Transconductance Amplifier (FCOTA) with evolutionary algorithm based synthesis methodology. Here, MOS transistor area is aimed to be minimized in such a way that power dissipation would be less and gain would be maximum in short computation time while satisfying the design specifications and design constraints.

This method uses a program based on Simplex-PSO optimization method to calculate the optimal transistors' dimensions, length (L), and width (W) for the CMOS TSC and CMOS FCOTA, which are used as parts of an electronic front-end for signal shaping stage. The design flow for both the CMOS TSC and FCOTA are shown in Fig. 1.

The remaining part of this work is organized as follows: In Section 2, described the design procedures of the Two-Stage Comparator and Folded Cascode OTA structures. In Section 3, Nedler–Mead Simplex method (NMSM) and Simplex-PSO method are briefly discussed for CMOS analog integrated circuit (IC) design. In Section 4, comprehensive and demonstrative sets of results are validated with CADENCE (IC 5.10) simulator. Finally, Section 5 concludes the paper

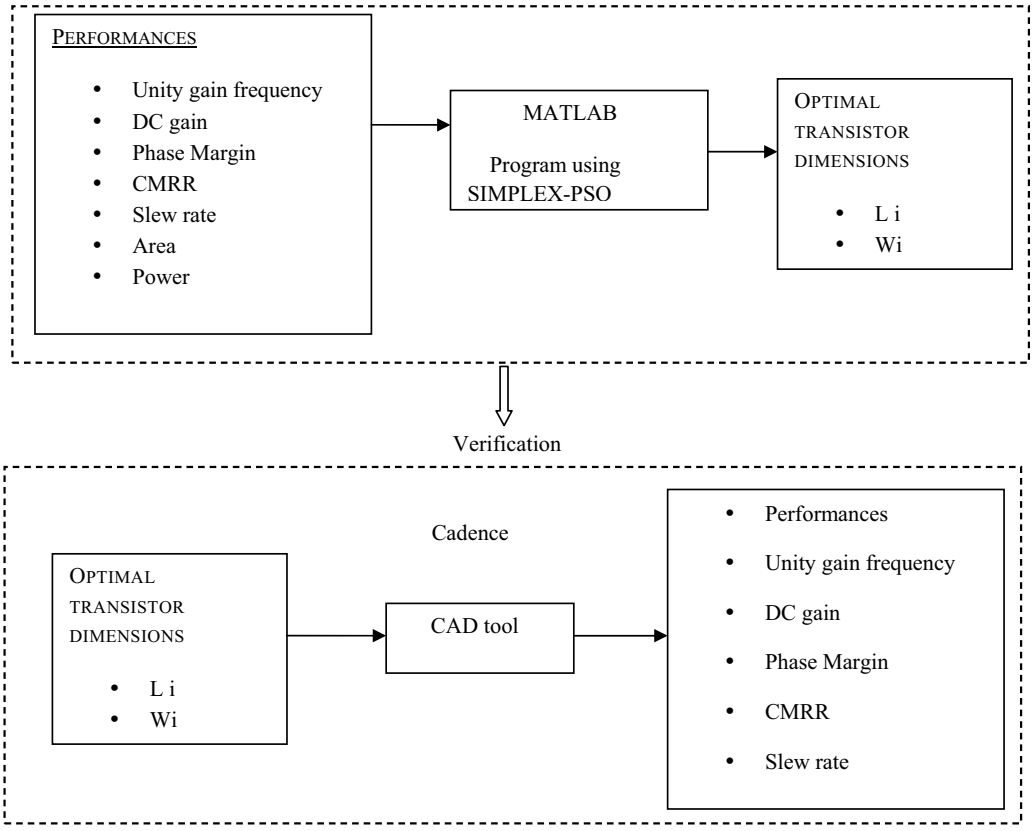

Fig. 1. Design flow for CMOS TSC and CMOS FCOTA.