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# Zero-power mismatch-independent digital to analog converter

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ABSTRACT

A new switched-capacitor digital to analog converter (DAC) is presented. In this DAC, a ladder of series capacitors is used to generate the output voltage levels. A correction phase is used to increase the precision of the DAC. It is analytically shown that the proposed DAC is mismatch independent by virtue of the correction phase. That is after few correction phases (typically one), the effect of mismatch on the reference voltage levels on the ladder diminishes and an accurate voltage division is provided. It is proven that the whole process sinks no extra charge from the power supply. Furthermore, post layout simulations in 0.18 μm technology proves the benefits of the proposed method.



## 1. Introduction

Nowadays, the capacitive DAC is used more than the other types of DACs because of three features: the capacitive DAC does not consume static power, it is robust to environmental changes such as temperature, and the precision of on-chip capacitors is well sufficient for high resolution ADCs. Although, conventional binary weighted DAC is precise, it occupies large area and consumes significant amount of energy. A binary weighted DAC with attenuation capacitor is proposed to reduce the area and power cost of the conventional binary weighted DAC [1], however, this structure has an inferior precision when the capacitor mismatch exists. C-2c structure is proposed to cover the area and power consumption problems of the two previous structures [2]. C-2c structure is more area and power efficient than the other DACs but it is prone to the effect of bottom plate capacitor and mismatch [3]. The problem of the mismatch effect was serious enough to give a superiority to binary weighted DAC than the other structures of the capacitive DACs for many applications.

Recently, a great effort has been made on binary weighted structure to reduce its power consumption. It is shown that by splitting the MSB capacitor the power consumption is reduce by 37% compared to the conventional binary weighted DAC [4]. The monotonic switching method was used in a 10-bit SAR ADC and reduces the DAC power consumption by 81% [5]. The tri-level method was proposed to further reduce power consumption. In this method, the power consumption is reduced by 96.89% by using the common mode voltage ($V_{cm}$) along with a reference voltage ($V_{ref}$) [6]. As an other case, the $V_{cm}$ based method achieves 97.66% power reduction [8].

Although, all of these works target the power reduction of the DAC, they do not consider the effect of capacitor mismatch in their works. This paper presents a new switching method which decouples the voltage levels generated by the DAC from any mismatch level of its components (capacitors). This paper is organized as follows. Section 2 presents the proposed circuit and correction phase. In Section 3, it is analytically shown that the proposed DAC is mismatch and process independent. Also, the convergence speed of the correction phase is discussed. Section 4 presents MATLAB and post layout simulation results. In Section 5 the power consumption is discussed. Section 6 concludes the paper.

## 2. The proposed idea

### 2.1. The proposed circuit

The proposed idea is shown in Fig. 1a which is based on a simple capacitor ladder. All capacitors are equal and initially discharged to zero volt. After connecting the positive terminal of the top capacitor to *Vdd* all node voltages settle at reference level values. Under ideal condition, where are capacitors are equal we have:

$$e_n = \frac{\frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n}}{\frac{1}{C_1} + \cdots + \frac{1}{C_n} + \cdots + \frac{1}{C_N}} \times Vdd = \frac{n \times \frac{1}{C}}{N \times \frac{1}{C}} \times Vdd = \frac{n}{N} \times Vdd \quad (1)$$

$N$ represents the number of capacitors and $e_n$ represents the steady-state voltage at node $n$. A binary code is applied to a multiplexer to direct the desired voltage level to the output as shown in Fig. 1b,c.

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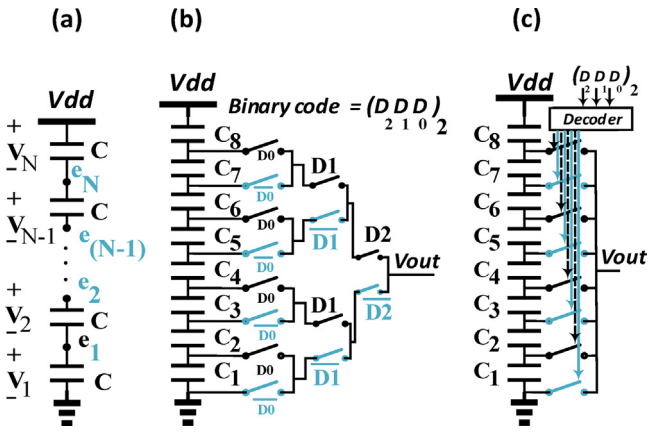


**Fig. 1.** (a) The proposed DAC, (b,c) two different structures to select output voltage level.

### 2.2. Correction phase

Owing to the switching, the initial voltage of the capacitors could be different. A correction phase is used to level the capacitor voltages. The correction phase for a typical 2-bit DAC is illustrated in Fig. 2. During the correction phase the positive terminals of all capacitors are connected to each other as well as the negative terminals. Thus, we have:

$$V_{1_{new}} = V_{2_{new}} = \cdots = V_{n_{new}} \tag{2}$$

Since all capacitors appear in parallel. The final voltage of the capacitors is calculated as follows:

$$C_1 = C_2 = \cdots = C_N \quad , \quad \mathbf{V_1} + \cdots + \mathbf{V_N} = \mathbf{Vdd} \tag{3}$$

$$V_{1_{new}} = \frac{C_1 \times V_1 + \cdots + C_n \times V_n}{C + C + \cdots + C} = \frac{C \times (V_1 + \cdots + V_n)}{C \times N} = \frac{Vdd}{N} \tag{4}$$

As a case study, Fig. 2 presents a typical 2-bit DAC and the voltage of nodes (Fig. 2b) before, during, and after the correction phase. The power consumption of the correction phase is zero because before and after the correction phase the sum of capacitor voltages is equal to *Vdd*. Therefore, the current drawn from *Vdd* is zero. Fig. 2c presents the effect of the correction phase on the voltage of the capacitors. All capacitors sustain the same voltage level after the correction is made. In the proposed method, whenever the capacitors are connected to *Vdd* the voltage levels are used as the output

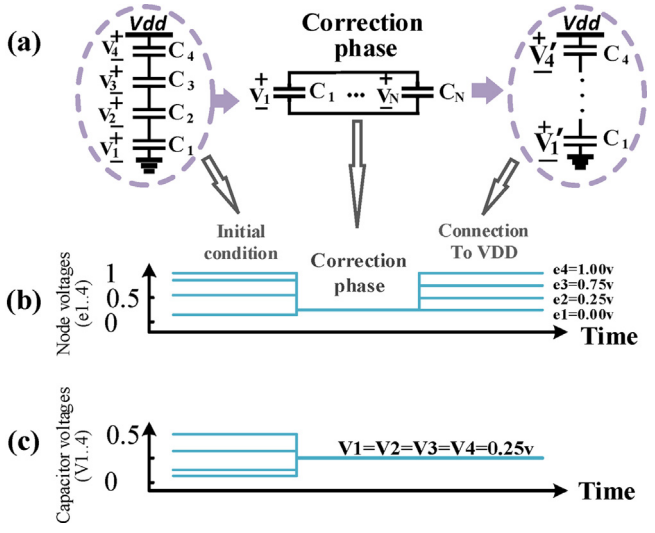


**Fig. 2.** Correction phase of proposed DAC.

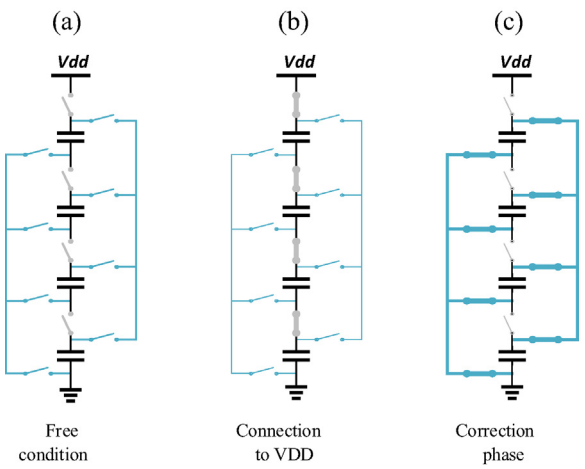


**Fig. 3.** The switching procedure of the proposed DAC, (a) free condition, (b) connection to *Vdd*, and (c) correction phase.

voltage of the DAC. After every conversion of the Analog to Digital Converter (ADC) the correction phase is made to level the reference voltages.

The switching structure to perform the series connection to *Vdd* and correction phase of the DAC is shown in Fig. 3(a). In this figure, central switches are used to place the capacitors in series with *Vdd*, as shown in Fig. 3b. The switches at right/left sides of the DAC perform the correction phase (Fig. 3c). The sizing of the switches is designed as shown in Fig. 4. In this structure, the time constant ($\tau$) of the connection to *Vdd* and correction phase circuits is the same as *RC*. As a result, the whole switching procedure of the DAC can be implemented using only one clock signal instead of DLL (delay lock loop) clock signals.

## 3. Mismatch and process variation independency

The correction phase makes the intermediate voltage levels resilient against the mismatch of the capacitors. Owing to the mismatch, the initial connection of the capacitor ladder to the *Vdd*, creates different voltage levels over the capacitors depending on their capacitance values. Once the capacitors go to the correction phase, where all capacitors are connected in parallel, the common equal voltage $V[k]$ is created over the capacitors (Fig. 2b). After this phase, the capacitors are placed in series with *Vdd* again (Fig. 2c). The voltage of the capacitors are different and equal to $v_{1\ldots N}$ because of the capacitor mismatch, where $v_i$ is calculated as follows:

$$v_n = V[k] + (Vdd - N \times V[k])\alpha_n \,, \quad \alpha_n = \frac{\frac{1}{C_n}}{\frac{1}{C_1} + \cdots + \frac{1}{C_n}} \tag{5}$$

At the next correction phase, a new common equal voltage level, $V[k+1]$, is created on the capacitors:

$$V[k+1] = \frac{v_1 C_1 + \cdots + v_N C_N}{C_1 + \cdots + C_N} \tag{6}$$

$$V[k+1] = \frac{[V[k] + (Vdd - NV[k])\alpha_1]C_1 + \cdots + [V[k] + (Vdd - NV[k])\alpha_N]C_N}{C_1 + \cdots + C_N} \tag{7}$$

Substituting $\alpha$ and factoring out $h$ which is defined as 9 yields:

$$V[k+1] = \frac{Nh(Vdd - NV[k])}{C_1 + \cdots + C_N} + V[k] \tag{8}$$

$$h = \frac{1}{\frac{1}{C_1}, \ldots, \frac{1}{C_N}} \tag{9}$$

Since the circuit does not include an inductor, it is a convergent periodic time variant system. At the steady-state condition, the