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Symbolic nodal analysis of conveyor-based circuits considering non-ideal active devices

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ABSTRACT

The nullor–mirror pathological elements have shown advantages in analog behavioral modeling and circuit synthesis. They can be employed to formulate the system of equations for symbolic nodal analysis. This paper presents a systematic analytical technique that performs nodal analysis of nullor–mirror circuits with the consideration of non-ideal active devices. By adding terminal parasitics to the available ideal nullor–mirror equivalents, the non-ideal active device models for the systematic analytical technique can be obtained. The application of the proposed technique to practical circuits is given to demonstrate the feasibility of the proposed method.

1. Introduction

Symbolic analysis is a systematic analytical technique which to calculate the behavior or characteristics of a circuit in terms of symbolic variables. It is a powerful tool for the analysis of electronic circuits to gain insight into the behavior of circuits [1–4]. Due to the convenience of performing symbolic analysis by applying only nodal analysis (NA), the pathological nullor elements are often used to model active devices [5–19]. In 1999, new pathological mirror elements were defined [20]. The mirror elements are conducive to representing active devices with reduced circuit complexity in comparison with their nullor representations. The simpler pathological nullor–mirror representations were further used in performing symbolic NA to improve the analytical efficiency [21,22]. Compared with the nodal admittance matrix formulation using the limit-variables method that a limit to infinity is always required to simplify the symbolic expressions and the solution of the system of equations is more complex, the symbolic NA using pathological element-based models achieves a considerable reductions in the order of the system of equations and in the generation of nonzero coefficients into the nodal admittance matrix [22,23]. However, most papers in literature considered the pathological representations of ideal active devices [7,24–28]. Only a few articles reported the pathological models of active devices including the non-ideal effects for symbolic analysis [6,22,29–31]. In [6,22], some pathological equivalents of active devices containing terminal parasitic effects were proposed but the non-unity current or voltage conveying gains were not included. In [29–31], the pathological equivalents of current mirror (CM) and voltage mirror (VM) with multi-outputs were proposed for symbolic analysis with the consideration of non-ideal effects. The reported equivalents include the input and output parasitics and non-unity current or voltage conveying gains. However, the presented pathological equivalents possess higher circuit complexities and additional effort must be paid to figure out the unavailable pathological models of non-ideal active devices. In this article, we present a convenient method to perform symbolic nodal analysis with the consideration of non-ideal active devices. The non-ideal active device models with simple structure for the proposed analytical method can be constructed easily. Due to the used model with reduced component and node numbers, the analytical efficiency can be enhanced. The feasibility and validity are illustrated by two representative circuits and the non-ideal signal source effect can be included.

2. Preparing realistic models for symbolic analysis

The VM and CM pathological elements are lossless two-port network elements and they are respectively used to represent an ideal voltage reversing property and an ideal current reversing property [20,32]. Each of the pathological mirror elements can be used as a bi-directional two-terminal component and adopted to model the behavior of many ideal active devices with compact structure for circuit analysis and synthesis [24–28,30,31]. Table 1 shows the

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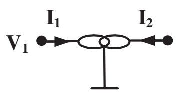
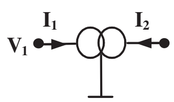
Table 1
Symbols and definitions of nullor and mirror elements.

(a)	Nullator		$V_1 = V_2$ $I_1 = I_2 = 0$
(b)	Norator		$V_1 - V_2 =$ arbitrary $I_1 = -I_2 =$ arbitrary
(c)	Voltage mirror		$V_1 = -V_2$ $I_1 = I_2 = 0$
(d)	Current mirror		$V_1 - V_2 =$ arbitrary $I_1 = I_2 =$ arbitrary

pathological nullor and mirror elements. Many nullor–mirror representations of ideal active devices are available in literature.

The symbols, device properties and pathological representations of some ideal active devices [27,33] are given in Table 2. It must be noted that all the current or voltage conveying gains of ideal active devices are unity so they are represented by the pathological elements. To consider the non-ideal (non-unity) current or voltage conveying gains of active devices in Table 2, the practical terminal voltage and current of the active devices can be observed and marked with blue words. Besides, the models in Table 2 will become more realistic if the input and output parasitic effects were included [22,30,34,35]. For instance, Table 3 shows the models of ICCII+, ICCII−, DXCCII and CDBA including parasitic effects. The blue labels in Table 3 are used to represent the practical current or voltage conveying gains. They are obtained in accordance with the terminal properties of active devices [34]. Similar treatment can be applied to other active devices to obtain their realistic models for symbolic analysis [22]. It should be noted that the above presented realistic models are simpler compared to the proposed models in [29], which at least needs the adding of one additional resistor and node to model each non-unity conveying gain.

3. Symbolic NA considering the non-ideal effects of active devices

The symbolic NA is an extension of passive nodal analysis [32] and involves the symbolic NA of an arbitrary interconnection of RLC–nullor–mirror networks and independent current sources in an $(N+1)$ node network. To perform symbolic NA considering the non-ideal effects of active devices, the active devices in the circuit should be replaced by their realistic models obtained using the method in Section 2. The analytic procedure of a nullor–mirror equivalent circuit can be described as below.

Step 1: For the $(N+1)$ node network, select a ground node and label all other nodes from 1 to N and denote the current flow through each of norators and CMs if it has not been denoted yet. Remember that no current flows through the nullators and voltage mirrors of the network.

Step 2: Write the $(N \times N)$ nodal admittance equations in matrix form:

$$\mathbf{I} = \mathbf{Y}_{N\times N}\mathbf{V} \quad (1)$$

$\mathbf{I} = \{I_1, I_2, \ldots, I_N\}'$, where the ith component I_i is defined as the sum of the currents flowing into the ith node from the independent current sources, norators or current mirrors. $\mathbf{Y}_{N\times N}$ is the passive nodal admittance matrix. Furthermore, $\mathbf{V}$ is the unknown column vector $\{V_1, V_2, \ldots, V_N\}'$ of node voltages.

Step 3: For a nullator that is connected between the nodes p and q, for example, one assumes that there is a voltage dependence between these two nodes, such as $V_q = \beta_1 V_p$ (β_1 represents the voltage conveying gain). Multiply the elements of column q of $\mathbf{Y}$ by β_1 factor then add the elements to the elements of column p and delete column q of $\mathbf{Y}$. If q is the ground node, simply delete column p of $\mathbf{Y}$. Thus, each nullator will cause the number of columns of the nodal admittance matrix $\mathbf{Y}$ to be reduced by one.

Step 4: For a VM that is connected between the nodes r and s, for example, one assumes that there is a voltage dependence between these two nodes, such as $V_s = -\beta_2 V_r$ ($-\beta_2$ represents the voltage conveying gain). Multiply the elements of column s of $\mathbf{Y}$ by $(-\beta_2)$ factor then add the elements to the elements of column r and delete column s of $\mathbf{Y}$. If s is the ground node, simply delete column r of $\mathbf{Y}$. Therefore, each VM will cause the number of columns of the nodal admittance matrix $\mathbf{Y}$ to be reduced by one.

Step 5: For a norator that is connected between terminals l and m, for example, one assumes that there is a current dependence between these two terminals, such as $I_m = -\alpha_1 I_l$ ($-\alpha_1$ represents the current conveying gain). Add (α_1) times the elements of row l of $\mathbf{Y}$ to the elements of row m, and delete row l. If m is the ground node, simply delete row l of $\mathbf{Y}$. Hence, each nullator will cause the number of rows of the nodal admittance matrix $\mathbf{Y}$ to be reduced by one.

Step 6: For a CM that is connected between the terminals n and o, for example, one assumes that there is a current dependence between these two terminals, such as $I_o = \alpha_2 I_n$ (α_2 represents the current conveying gain). Add $(-\alpha_2)$ times the elements of row n of $\mathbf{Y}$ to the elements of row o, and delete row n. If o is the ground node, simply delete row n of $\mathbf{Y}$. Hence, each CM will cause the number of rows of the nodal admittance matrix $\mathbf{Y}$ to be reduced by one.

Step 7: The preceding steps result in the reduction of the $(N \times N)$ nodal admittance matrix of the original network to the $(N-K-L) \times (N-K-L)$ nodal admittance matrix. The corresponding $(N-K-L)$ equations may be solved for the independent node voltages. $(K+L)$ is the number of nullators (or VMs) and norators (or CMs) pairs [23]. It must be noticed that each of the voltage or current conveying gains of active devices mentioned above can be either a constant which represents the low-frequency conveying gain or a conveying function which contains the frequency response characteristic [35]. For example, a conveying function can be expressed as $\beta_1/(1+s/\omega_p)$ where β_1 is the low-frequency conveying gain and ω_p denotes the dominant pole.

4. Application examples

To demonstrate the feasibility of the proposed symbolic NA technique in Section 3, two representative circuit examples are illustrated. Firstly, we takes into account the ICCII+-based voltage-mode lowpass filter in [36] for comparison with previous symbolic NA technique. It is the same circuit as the filter in Fig. 5 of [29]. Using the realistic model of the ICCII+ in Table 3(a), the nullor–mirror representation of this filter is redrawn in Fig. 1, with the inputted