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Design and analysis of DC gain and transconductance boosted recycling folded cascode OTA

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ABSTRACT

A new technique for improving the transconductance and low frequency output impedance of recycling folded cascode (RFC) amplifiers is presented. This enhancement was achieved by using a positive feedback and upgrading the recycling structure. The new structure profits from better transconductance, slew rate, and DC gain in comparison with conventional folded cascode (FC) amplifier. Moreover, the input referred noise is reduced and the phase-margin improved. The enhanced amplifier, simulated in 0.18 μm CMOS technology, exhibits a DC gain enhancement of 16.3 dB as well as 115.5 MHz increase in gain bandwidth compared to conventional FC configuration. The amplifier consumes 360 μW @ 1.2 V which makes it suitable for low-voltage applications.

1. Introduction

The advancement of CMOS technologies has improved the growing market of mobile and portable electronic devices. This is achieved by the continual integration of complex analog and digital building blocks on a single chip. As a result, Silicon area and power consumption have emerged as key parameters to consider for successful design [1].

Because of their high gain and speed, folded cascode (FC) operational transconductance amplifiers (OTAs) play a central role in many analog systems. However, their large die area and high power consumption are limiting their use in mobile and portable systems. With its higher gain and bandwidth over conventional FC amplifier, the recycling folded cascode (RFC) configuration was introduced to address these issues. However, the RFC amplifier has an extra pole-zero pair which leads to decay in the phase-margin [1–3]. Recent works on RFC include phase-margin network [4], positive feedback [5], or extra current sources [6] to enhance performance of RFC amplifiers. In the two last approaches, the transconductance is increased without consuming more power. However, the enhancement in transconductance is counterbalanced by a serious degradation in the phase-margin, leading to unstable behavior in the amplifier. The double recycling technique uses extra shunt current sources added to the input stage to recycle the bias current once again [6]. In addition, the positive feedback can be used for increasing the output impedance, leading to higher transconductance and low frequency output impedance [7,8].

In this paper, an enhanced low-voltage RFC amplifier with a high-speed current mirror is presented. It presents an improved transconductance, DC gain, slew rate and phase-margin over existing RFC devices. Furthermore, the input referred noise is decreased through a transconductance enhancement. The paper is organized as follows. In Section 2, a brief description of recycling folded cascode amplifiers is provided. Then in Section 3, a theoretical analysis is given for transconductance, DC gain, slew rate, phase-margin and noise. Simulation results and conclusion are presented in the last section.

2. Conventional recycling structures

Conventional configurations of FC and RFC amplifiers are shown in Figs. 1 and 2, respectively. Compared to FC, RFC amplifier utilizes M3 and M4 as driving transistors [1,3]. Moreover, the input drivers (M1, M2) are divided into Ma1, Ma2 and Mb1, Mb2, with equal current flow of $I/2$ (Fig. 2). Also, the cross-over connections of current mirrors Ma3:Mb3 and Ma4:Mb4 ensure that the small signal current is amplified by a ratio factor k. Therefore, the operative transconductance (Gm) of the RFC can be expressed as

$$Gm_{RFC} = gm_{a1}\,(1+k) \tag{1}$$

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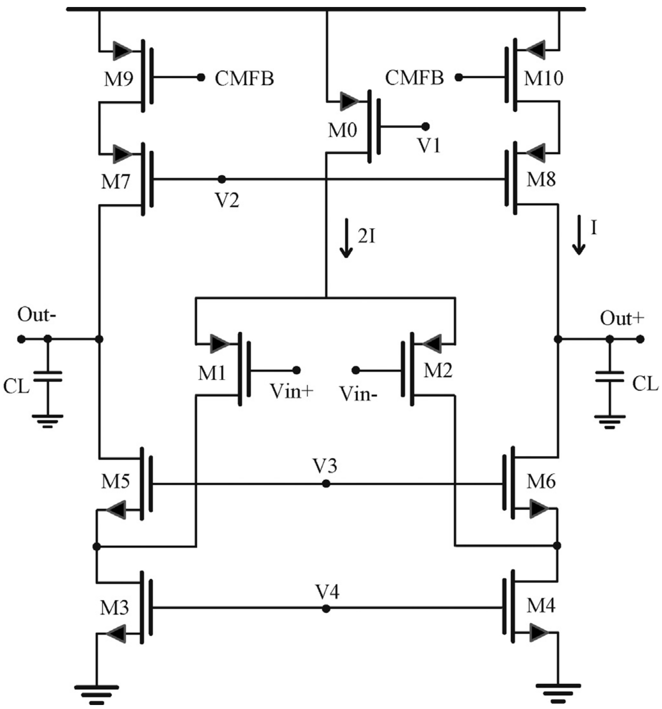

Fig. 1. Schematic of conventional folded cascode amplifier.

Despite the fact that the gain bandwidth (GBW) product is increased due to transconductance enhancement, the phase-margin is degraded by the large value of k ratio. In other words, improvement in transconductance is limited by phase-margin degradation. Usually, a value $k = 3$ allows maintaining the power budget unchanged. Thus, the transconductance of the RFC is twice that of the FC, and consequently twice the GBW [1,4].

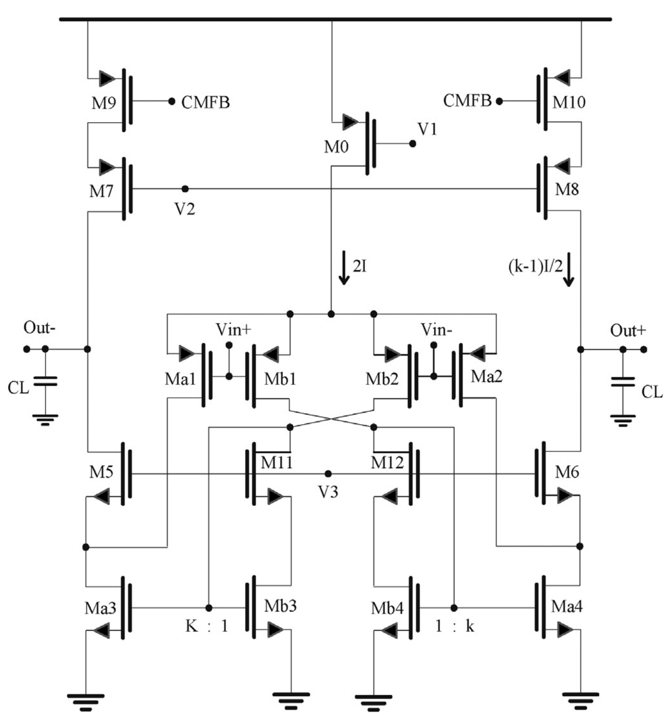

Fig. 2. Schematic of recycling folded cascode amplifier.

3. Architecture of the enhanced RFC amplifier

The enhanced recycling folded cascode (ERFC) amplifier is presented in Fig. 3. Note that transistors M9 and M10 conduct a large current value; thus, can exhibit large transconductance. Therefore, besides the M3 and M4 in RFC, M9 and M10 in ERFC are involved in input drive. In order to use M9 and M10 as driving transistors, the cross-over connections of current mirrors Mb3:M9 and Mb4:M10 ensure that the small signal current is amplified by a ratio factor $(k-1)$ (the signal being injected into the gate of M9 and M10 through these current mirrors). To maintain the amplifier as a double-ended architecture with common mode feedback circuit, M11 and M12 are added to conduct the current value of $[(k-1)/10]I$. Increasing the currents in M11 and M12 leads to a decrease in currents in M9 and M10, which in turn decreases the corresponding transconductance. As a result, the currents in M11 and M12 need to be lower than that in M9 and M10 as long as it does not affect the functionality of the circuit.

Finally, M13 and M14 maintain equal drain potentials across Ma3:Mb3 and Ma4:Mb4 for improved matching. These modifications provide the ERFC with enhanced features over that of FC and RFC.

In order to quantitatively present these enhancements, all devices are assumed to operate in the strong inversion region following the simplified square-law drain current model expressed by

$$Id = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (2)$$

Here all symbols have their usual meanings [1].

3.1. Small signal transconductance

The amplifier's transconductance (Gm) is obtained by calculating the short-circuit current at the output with regards to the input. Because M1 is twice the size of Ma1, it conducts twice current, thus $gm_1 = 2gm_{a1}$. Also, the current gain k shown in Fig. 3 is selected equal to 3 to keep same power consumption and area. Therefore, the ERFC has 200% and 50% improvement in transconductance compared to the FC and RFC, respectively. Also, for the same amount of power, the ERFC gain-bandwidth (GBW) product is increased by a factor of 3 compared to that of the FC. Small signal transconductance for FC and ERFC are expressed in (3) and (4).

$$Gm_{FC} = gm_1 \quad (3)$$

$$Gm_{ERFC} = gm_{a1}(2k) \quad (4)$$

3.2. DC gain

The DC gain of transconductance amplifiers is usually described as the product of the small signal transconductance, Gm, with the low frequency output impedance, $Rout$. Thus, enhancing transconductance and increasing the output impedance should boost the DC gain. As shown in Fig. 3, the positive feedback structure in the ERFC amplifier is created by connecting the gate terminal of cascode transistors M7 and M8 to the folded nodes. In fact, in order to make positive feedback (i.e., phase difference of 180°), the gates of M7 and M8 need to be connected to folded nodes (Fig. 4), which, consequently, almost double the output impedance. However; this will affect the amplifier linearity and output voltage swing. It should be noted that the positive feedback used in this paper is different from the ones in [7,8]. Indeed, in those feedback structures, the stability criteria should be checked out while in the proposed structure, the output impedance is always positive (because the currents of M5–M8 are all the same), thus leading to a stable circuit.