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Extraction of small-signal equivalent circuit model parameters for Si/SiGe HBT using *S*-parameters measurements and one geometrical information

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Abstract

A physical and simple method is proposed to extract the hybrid-π small-signal equivalent circuit model of Si/SiGe heterojunction bipolar transistor (HBT). In this method, we use test (dummy) structures to extract by means of fitting techniques the extrinsic bias-independent parameters representing the contact pads plus the transmission line connections to the core of the active device. All intrinsic bias-dependent parameters are calculated analytically from *S*-parameters only. The ratio of the area of the emitter contact to base area is used to solve the base–collector feedback problem due to the distributed nature of the base. Using this physical (geometry) constraint instead of the measured direct current (DC) information helps to get more reliable parameters and easier calculations. When we applied this methodology, a good agreement is obtained between the modelled *S*-parameters with the corresponding measured ones over the broad band from 40 MHz to 20.02 GHz. The error for three different bias points was less than 1.2%.

Keywords: Heterojunction bipolar transistors; Microwave devices; Modeling

1. Introduction

There is a high demand for Si/SiGe heterojunction bipolar transistors (HBTs) in the area of Si-based microwave monolithic microwave integrated circuits (MMICs) due to their superior high-frequency performance [1]. For the design of MMICs, an accurate model needs to be developed. The most common models for HBTs are compact models such as VBIC, HICUM, and MEXTRAM [2,3]. The general drawback of compact models is the difficulty to extract their parameters, as many kinds of measurements and setups are required for this purpose. For this reason, we prefer the equivalent scheme approach. The extraction consists of two steps: the extraction of the external pad and transmission line parasitic, and the extraction of the intrinsic device parameters. Concerning the former, the network representing the pad and transmission line parasitics is more complicated in case of Si-based devices than in case of III–V based devices due to the lossy behaviour of Si substrate. For this reason, we cannot use the available published works [4–7] which are used to extract III–V device models. Concerning the extraction of the intrinsic parameters, we will neither use any extra direct current (DC) information nor numerical optimization techniques, as the authors of the previously mentioned works did.

The paper is organized as follows: In the next section, the extraction of the pad and transmission line parasitics is presented. The derivation of the analytical expressions used to obtain the intrinsic parameters is elaborated in the following section. We validate the accuracy of the obtained model using vector network analyser (VNA) measurements in the penultimate section. Finally, the conclusions are drawn in the last section.

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2. Extraction of parasitic elements

The complete small-signal equivalent circuit for a Si/SiGe HBT as seen from the probe tips is shown in Fig. 1. We distinguish two parts: the intrinsic core of the device and the external parasitics. In this section, we concentrate on the parasitics, while the extraction of the intrinsic elements is discussed in the next section. Concerning the parasitics, we can deduce three types from Fig. 1: pad parasitics, impedance or series parasitics of the access transmission lines, and admittance or parallel parasitics of the access transmission lines. The first step in the extraction procedure is to subtract the effects of these parasitics. If we apply the well-known technique used for extracting the parasitics of III–V device models [7], we have to bias the device in special settings, being saturation (to extract the inductive and resistive parasitics) and cut-off (to extract the capacitive parasitics). Some problem arises from the work in saturation mode, where the method assumes that at high I_B (base current) the low junction dynamic resistances will short-circuit the junction capacitances, and therefore that the imaginary parts of Z-parameters of the equivalent circuit are dominated by the inductances of the device. In case of our device, this condition is difficult to obtain. Also, we found that in cut-off mode the equivalent circuit is not purely capacitive due to the Si substrate. So it is impossible to extract the capacitive parasitics.

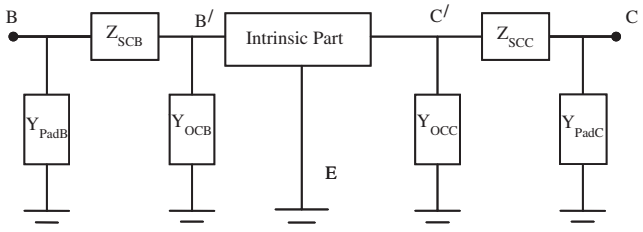

Fig. 1. Representation of the Si/SiGe HBT in the measurement configuration. The actual transistor is represented by the rectangle called 'intrinsic transistor'. The series impedances and parallel admittances model the probe pads and access transmission lines.

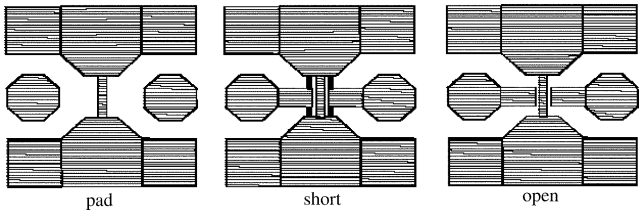

Fig. 2. Pad, short-circuit, and open-circuit dummy structures.

A possible alternative solution is to first find an equivalent circuit for the pad and access transmission lines, as shown in Fig. 2. This technique was applied in [8] for AlGaAs/GaAs HBT. Due to the isolating properties of III–V materials the proposed circuits for the dummy structures are much simpler than in our case where we are considering a Si/SiGe HBT. These simple circuits allow the authors of [8] to extract the circuits parameters with a direct extraction method without need for any optimization routines. The equivalent circuits we propose for each of the dummy structures are shown in Fig. 3. They are built on the same concept as in [9]. As the topologies of the base–emitter and collector–emitter networks are identical, only the former is shown. The complexity of the circuits comes from the dispersive nature of the Si substrate. Note that we are supposing that $S_{12}=S_{21}=0$ for all dummy structures. This can be justified as follows:

In case of the pad and open-circuit dummy structures, there is a negligible physical path between base and collector through the substrate. Also, as the transmission through is very short and the frequencies we are considering (up to 20 GHz) are still relatively low, we decided to neglect it. Finally, in case of the short-circuit dummy structure, it is clear that there is no transmission between the input and output. The element values of these parasitic networks have been obtained by a random search optimization method. This optimizer-based parameter extraction method involves that numerical search algorithms are used to minimize the error between the measured and simulated S-parameters.

3. Modelling of the intrinsic core

In the previous step, we have built a model for the pad and access transmission lines. The present step concerns the modelling of the intrinsic core of the HBT as shown in Fig. 4 [7]. This equivalent circuit contains seven elements

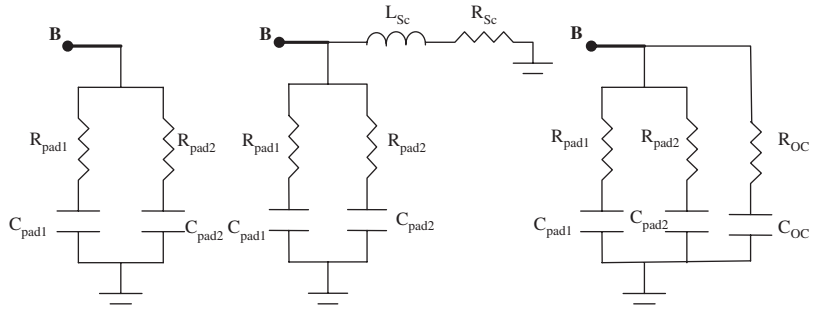

Fig. 3. Equivalent circuits of (a) pad, (b) short-circuit, and (c) open-circuit dummy structures in the case of Si/SiGe HBT.