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Differential current conveyor based current comparator

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ABSTRACT

A New differential current conveyor based current comparator is presented in this paper. Differential current conveyor II (DCCII) is designed, modified, and exploited as a comparator with reduced propagation delay and power consumption. New DCCII decreases propagation delay and increases comparator accuracy considerably. Simulation results using Hspice and 0.18 μm CMOS technology with 1.8V supply voltage confirms a less than 0.63 ns propagation delay at ±1 μA input current. Average power dissipation in ±1 μA input current has a value of 300 μW.

1. Introduction

Comparators are most significant part of analog integrated circuits after operational amplifiers [1,2]. Current mode approach advantages lead to current comparator interest in integrated circuit. Moreover, current conveyor could act as an Op-Amp in current mode approach. Sedra and Smith in 1968 presented the first generation of current conveyor (CCI) [3]. The second generation current conveyor (CCII) was presented in 1970 by them [4]. However, a certain work to determine that the current conveyor was a more advantageous device than the operational amplifier, could not be done during following ten years. Current mode approach in last decade has drawn lots of interest, as supply voltage of the circuits reduces. Second generation current conveyor (CCII) is one of the versatile current mode blocks. CCIIs have such a compatible configuration that many voltage mode blocks can be easily substitute by them. They show some drawbacks as it present only one high impedance input. Moreover, differential signals are often voltage or current; as a result, circuit need two low impedance or high impedance terminal respectively. Fig. 1a and b, demonstrate differential second generation current conveyor (DCCII) block and matrix characteristic, respectively [5]. Also, matrix characteristic results are shown as following equations:

$$I_{Z1} = I_{X1} - I_{X2} \quad (1)$$

$$I_{Z2} = I_{X2} - I_{X1} \quad (2)$$

$$V_{X1} = V_{X2} = V_Y \quad (3)$$

Current approach characteristics have more advantages than voltage mode [6,7]. Current comparators are essential block in data convertor circuits such as delta-sigma modulator A/D converters [8–10]. Furthermore, one of the data convertor bottlenecks is the speed limitation of the comparator; hence, any improvement in this area leads to a major enhancement in circuit operation and circuit could perform in higher frequency range. In an alternative approach, single ended current conveyor based comparator is used which input current compare instantaneous current with zero value [11].

This paper presents a conceivable approach for designing a low power, and high speed differential current mode comparator based on current conveyor (DCC-CCII). In part two circuit designs is described; while in section three simulation results are presented. The conclusion is given in Section 4.

2. Circuit design

The current comparator concept as expressed by Lin et al. [12] and shown in Fig. 2a is as follows; the input current is injected into input stage and is converted to the voltage V_{IN} and V_1 by amplifier *A1* and voltage buffer *A2*. V_1 is amplified using the high gain amplifier (*A3*) to generate the output logic voltage level. A modified DCCII is used as input stage of the new proposed current comparator due to the low input impedance at current nodes *X*1 and *X*2, and the inherent current to voltage conversion property of the DCCII circuit.

A wide number of DCCII topologies in different classes such as A, and AB are implemented in CMOS technology [13–18]. Some important design features that are used in most recent differential current conveyors are extracted and exploited to this circuit. In addition, modified DCCII should satisfy the characteristic matrix equations. Neglecting the mismatch effect of *M1–M4* transistors

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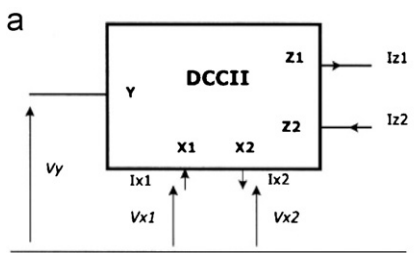

$$b\begin{pmatrix} V_{X1} \\ V_{X2} \\ I_{Z1} \\ I_{Z2} \\ I_Y \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 \\ +1 & -1 & 0 & 0 & 0 \\ -1 & +1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \\ V_Y \end{pmatrix}$$

Fig. 1. DCCII Block representation (a) and matrix characteristic of DCCII (b).

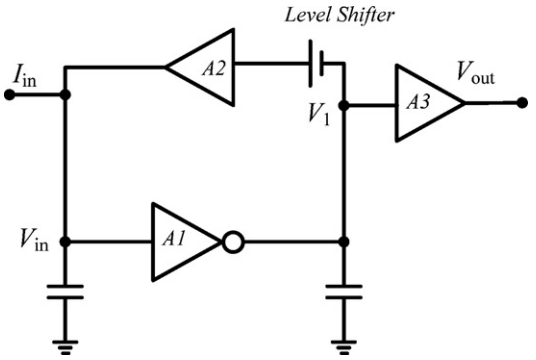

Fig. 2. Current comparator concept model.

could lead to equal gate-source voltages. As a case in this point, the unity voltage transfer function (V_X/V_Y, Eq. (3)) is ensured by using differential pair transistors *M1–M4*. Furthermore, for calculating the *X* terminal parasitic impedance common small signal model are used. Eqs. (4) and (5) are the exact and approximate amount of input impedance, respectively. Practically, bias conditions make the transconductance value about 500 μV/A and hence a 2 KΩ input impedance. The mentioned transconductance is justified by *M7–M8* and *M11–M12* transistors. Simulation result confirms this parasitic impedance. In addition, to obtain equal output impedances and full swing in low current two inverters are added to the *Z* terminals.

$$R_X = \frac{1}{g_{m7}} || r_{o7} || r_{o5} \tag{4}$$

$$R_X \cong \frac{1}{g_{m7}} \tag{5}$$

Due to a two gate stage design, the comparator could operate appropriately in low voltages applications. In addition, circuit could be enhanced by replacing ordinary current mirrors with Wilson current mirror and other alternative and prevalent current mirrors [19–21] to obtain accurate current copies and higher output impedances while low voltage operation decrease significantly. In order to unify output resistance, two inverters are added at the output stage. Therefore, output parasitic impedances are restricted by $r_o/2$ and boosted by enlarged transistor's length. The complete schematic of DCC-CCII is presented in Fig. 3.

Table 1
Transistors aspect ratios.

Transistors	W/L
M1–M4	0.36/0.18 μm
M5–M12	0.42/0.18 μm
M13–M16	0.72/0.36 μm
M17–M18	0.42/0.36 μm
M19–M20	0.72/0.36 μm

As can be seen in Fig. 3 input currents enter from *X*1 and *X*2 terminals and output senses from *Z*1. Transistor dimensions are shown in Table 1. According to previous discussion output transistors length should be increased with respect to other transistors since they determine the entire output impedance. Finally, bias current selection is a sort of trade off between power and speed. In this current mode circuit bias currents do not have a critical effect on the speed in contrast to voltage mode. So, all of the bias currents are selected to value of 5 μA.

3. Simulation results

In this part all of the required simulation such as transient, dynamic range and process variations of the proposed circuit is demonstrated. First, a 100 MHz differential input current signals with ±1 μA amplitude is conveyed and compared. Fig. 4 illustrates the transient input–output characteristics of the comparator, where a short propagation delay of approximately 0.6 ns is observed under mentioned input current. Hence, an input frequency of more than 400 MHz is now achievable. Power dissipation for various input currents is one of the characteristics of this circuit. The average power dissipation that is shown in Fig. 5a is calculated to be 300 μW. Furthermore, variations of propagation delay

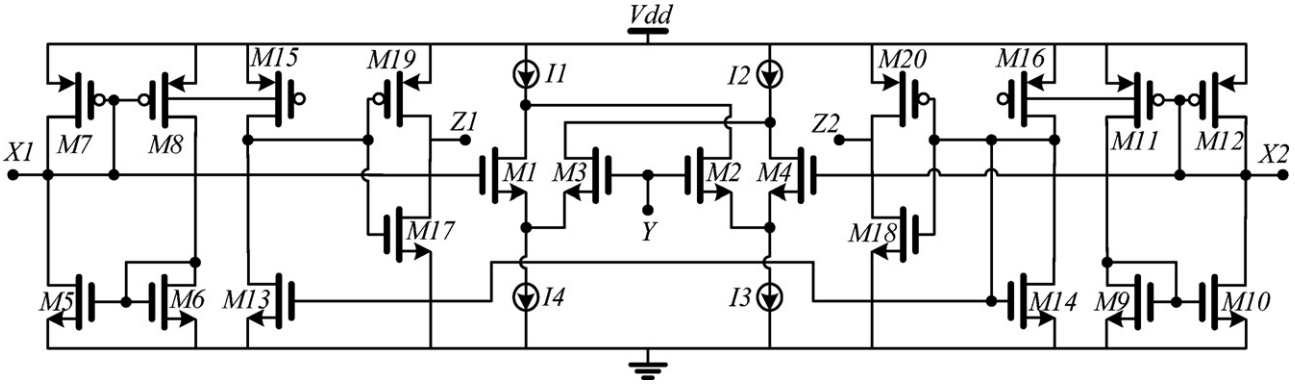

Fig. 3. Complete schematic of DCC-CCII.