



## Low-voltage high-gain large-capacitive-load amplifiers in 90-nm CMOS technology

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### ARTICLE INFO

#### Article history:

Received 5 August 2014

Accepted 8 December 2014

#### Keywords:

Multistage amplifier

Three-stage amplifier

Frequency compensation

Nested Miller compensation

Active feedback

### ABSTRACT

Low-voltage and low-power multistage operational transconductance amplifiers with new and efficient gain boosting and frequency compensation schemes are proposed in this paper. The presented amplifiers are designed to drive large capacitive loads with small power consumption at low-voltage supplies. The compensation schemes exploit a single Miller capacitor and an active feedback to form the main negative feedback loops for pole splitting and two feedforward paths. The new gain boosting technique discussed here improves the dc gain with negligible effect on the frequency response. The analysis and design procedures are discussed and the performance enhancements of the amplifiers are verified. The proposed OTAs have been implemented in a standard 90-nm CMOS process and the post-layout simulation results are reported. The amplifiers consume 8.7  $\mu$ W and 8.1  $\mu$ W at 0.5-V supplies and achieve 12.65 MHz and 2 MHz gain-bandwidth products while driving 150-pF and 15-nF capacitive loads, respectively.

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### 1. Introduction

Low-power operational amplifiers are required for a variety of applications especially battery-powered and handheld electronic equipments. With the continuous downscaling of channel length of transistor in CMOS technology, digital systems benefit from better integration and higher speed. To save the dynamic power and to alleviate the leakage of the transistors, the supply voltages for these circuits continue to scale down, too. For mixed-mode signal processing systems where analog and digital circuits co-exist, the design of analog modules poses many challenges [1–4].

The operational transconductance amplifier (OTA) is the core building block in analog systems. Lowering the supply voltage of amplifiers causes a drastic degradation in dc gain, because traditional cascode topologies can no longer be utilized [5–7]. Moreover, for nano-scale CMOS processes where transistors inherently suffer from low intrinsic gain, using a low supply voltage reduces the small signal drain-source resistance of the transistors and the gain is further exacerbated. On the other hand, high dc gain is essential for high precision purposes. The common solution is to cascade several gain stages [1–11]. In nano-scale technologies, numerous (for instance four) stages have to be used. Each gain stage introduces a high impedance node and adds a low frequency pole

resulting in a degraded stability. Therefore, to guarantee the stability more complex compensation techniques are required. Most of the frequency compensation topologies are based on nested Miller compensation (NMC) [12] method. The NMC amplifier has a good stability but it suffers from severe bandwidth reduction and large power consumption [1,8,10,13]. To alleviate these drawbacks, other topologies such as NMC with feedforward and nulling resistor (NMCFFNR) [13], reversed NMC (RNMC) [7], RNMC with feedforward and nulling resistor (RNMCFFNR) [5] were reported. Also, some advanced techniques use active feedbacks to create high speed paths and improve the bandwidth [1,8–10,14]. In order to further enhance the gain-bandwidth product, other techniques such as multipath NMC (MNMC) [15], impedance adapting compensation (IAC) [16], and no capacitor feedforward (NCF) [17], generate left half plane (LHP) zeros and perform pole-zero cancellations. The pole elimination improves the phase response and sufficient phase margin is possible with larger unity gain frequencies. However, doublets in the transfer function may cause small signal transient response degradation [18]. Besides, these doublets usually are placed in the pass-band and cause the more sensitivity of the settling time to process, voltage, and temperature (PVT) variations. Most of the methods discussed above are proposed for three stage amplifiers. For higher dc gains, four stage amplifiers are also reported. The four stage amplifiers in [3,19] use large capacitive feedbacks and large transconductors to push the non-dominant poles to higher frequencies and to get sufficient overall phase margin. Clearly, this leads to larger die area and higher power consumption.

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From the above it can be concluded that most of the frequency compensation methods for multistage amplifiers are either based on pole splitting that requires large compensation capacitors and cause bandwidth reduction, or they use in-band pole-zero cancellations which unfavorably affect the settling time. In this paper, new low-voltage, low-power, and high-gain amplifiers for driving large capacitive loads are proposed. The high dc gain is not obtained through cascading numerous high impedance nodes and the gain boosting has a marginal effect on the frequency response. Additionally, the OTA exploits new and efficient compensation techniques to ensure the stability while allowing higher gain-bandwidth products. The paper is organized as follows. In Section 2, the structures of the proposed amplifiers are introduced. The small-signal analysis, the stability considerations, and a simple design procedure of the amplifiers are discussed in Section 3. Section 4 presents the circuit level realizations of the amplifiers. The simulation results are provided in Section 5, and finally, Section 6 concludes the paper.

**2. Architectures of the proposed amplifiers**

In most of the conventional multistage amplifiers the first stage is either a telescopic or a folded cascode OTA and the rest of the circuit is composed of cascaded inverting and non-inverting common source amplifiers. These gain stages create high impedance nodes and low frequency poles which add negative phase shift to the phase response and degrade the overall phase margin that may lead to instability. In this paper to boost the dc gain without altering the frequency response, the structure of the intermediate stages has been modified. Here, instead of using the ordinary high impedance gain stages, the low impedance stages depicted in Fig. 1 have been utilized. The approximate voltage gain of the amplifiers shown in Fig. 1(a) and (b) are equal to  $g_{m1}/g_{m3}$  and  $(g_{m1} + g_{m2})/g_{m3}$ , respectively. Clearly, the amplifier shown in Fig. 1(b) is the more preferable option because it achieves about twice the gain of that suggested in Fig. 1(a). The drawback of these structures is that the conventional telescopic or folded cascode amplifiers cannot be used as the first stage because the quiescent current of transistor  $M_1$  is not well defined in the amplifiers depicted in Fig. 1. In other words, the gate of  $M_1$  should be connected to a current mirror instead of the high impedance output node of a telescopic or a folded cascode amplifier. Clearly, leaving out these high gain OTAs and replacing them with current mirrors results in a substantial gain reduction.

In order to overcome this drawback, for the first stage a modified folded cascode OTA is proposed and will be discussed in the following sections. The block diagram of the newly proposed low-voltage gain-boosted amplifier is shown in Fig. 2. The compensation network is made up of a single Miller capacitor and two feedforward paths (SMF).

The amplifier consists of seven amplifying stages. The first and the last stages are high-gain and the remaining five intermediate stages are low-gain low-impedance amplifiers. The transconductance, the parasitic capacitance, and the small signal output resistance of the  $i$ th stage are represented by  $g_{mi}$ ,  $C_i$ , and  $R_i$ ,

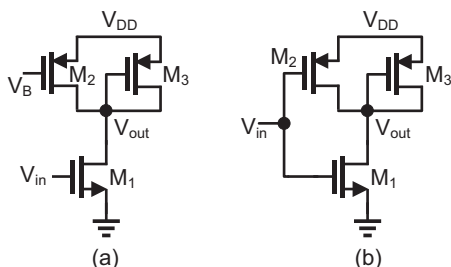


Fig. 1. Low-gain low-impedance amplifiers for intermediate stages.

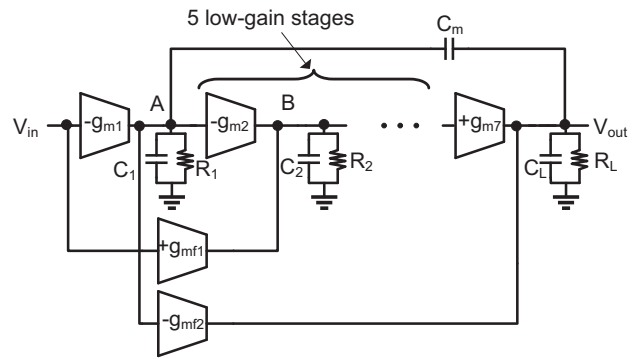


Fig. 2. The block diagram of the proposed amplifier with single Miller capacitor and feedforward paths (SMF).

respectively. The feedforward path with transconductance  $g_{mf1}$ , generates a left half plane (LHP) zero to compensate for the negative phase shift caused by non-dominant poles. The transconductance stage  $g_{mf2}$ , contributes to realizing a push-pull output stage which improves the large signal performance.

For some applications such as headphone and active matrix LCD drivers, the amplifiers should be able to drive capacitive loads of up to a few nano Farads [20]. For portable systems, the supply voltage and the power consumption should be kept low to minimize the die area and extend the battery life. Compensating the frequency response of such amplifiers is a more complicated task. To this end, the OTA shown in Fig. 3 which uses an active Miller feedback (AMF) is proposed.

The distinction of this amplifier (AMF) with the previously discussed one (SMF) is that the Miller capacitor has been replaced by a negative active Miller feedback and the feedforward transconductance,  $g_{mf1}$ , has been eliminated.

Herein, the design strategy is to replace the high gain intermediate stages or high-impedance nodes with several cascaded low-gain amplifiers or low-impedance nodes. In such a way, instead of having several low frequency poles associated with intermediate nodes (for instance two for four stage OTAs), there will be several high frequency poles because the time constant of each node ( $R_i C_i$ ) is reduced. These high frequency poles associated with the five intermediate stages should be placed at least 10 times the unity gain frequency to make sure that their overall negative phase shift is adequately small. Also, the first non-dominant pole is pushed to higher frequencies by applying pole-splitting task via a single Miller capacitor,  $C_m$ . The LHP zero generated by the transconductance  $g_{mf1}$ , is used to cancel the negative phase shift of the first non-dominant pole. Since this cancellation takes place beyond the unity gain frequency, its effect on the settling time is marginal [16]. The targeted pole-zero distributions are shown in Fig. 4.

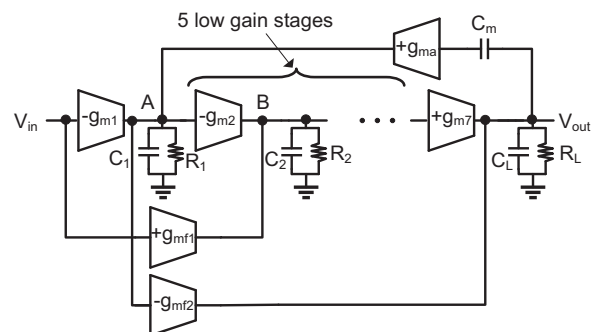


Fig. 3. The block diagram of the proposed heavy-load amplifier with active Miller feedback (AMF).

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