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Clock recovery based on packet inter-arrival time averaging

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Abstract

Accurate source clock recovery is an important element of circuit emulation services (CES) over packet networks. A well-known and widely implemented technique for clock recovery in CES is the one that is based on packet inter-arrival time (sometimes called time difference of arrival (TDOA)) averaging. The technique is very simple to implement but provides good performance only when packet losses and packet delay variation (PDV) are very low and well controlled. This technique has not been fully characterized analytically in the literature. In this paper, we provide a full analytical examination of this well-known clock recovery technique. We analyze the effects of correlation of the PDV experienced by the constant bit rate (CBR) traffic stream on the quality of the clock recovered by a receiver. We prove analytically that, for a general input process, high correlation of the PDV produces a large variance of the recovered clock. The paper also describes simple all-digital implementations of the clock recovery scheme using standard digitally controlled oscillators (DCOs).

Keywords: Circuit emulation; TDM; Clock recovery; Timing recovery; Clock synchronization; Phase-locked loop; Digitally controlled oscillator; DCO; Packet networks; Jitter; Packet delay variation; PDV

1. Introduction

Packet networks (e.g. IP, MPLS, Ethernet, etc.) are fast becoming an attractive alternative to circuit-switched networks since they offer higher efficiency when the network is used for many bursty data sources. They also carry significantly less capital investment for network equipment than their time division multiplexing (TDM) equivalent. Continuous bit stream (CBR) or TDM traffic, which is naturally conveyed over circuit-switched connections, must now be packetized before transmission and reconstructed into TDM bit stream at the receiver. The reconstruction process is complicated by variable network delays when the network is asynchronous or when a terminal operates on network independent timing. Frequency offsets between the transmitting and receiving terminals must be eliminated in order to avoid underrun or overrun at the receiver. This problem is readily solved in a TDM connection between the two terminals. For example, in the circuit switched network, a constant bit rate service such as a DS1 is usually synchronized to the network timing via pulse stuffing techniques. However, in a packet environment, the physical bit stream is very bursty and does not directly supply transmitter timing information. Random network delays as well as packet multiplexing also contribute significant variability to the packet arrival process.

Circuit emulation for TDM traffic over packet networks is receiving much attention nowadays [1–7]. A packet network that interconnects TDM devices must essentially behave as a transparent 'link' in the end-to-end TDM connection. This transparent inclusion of a packet network in an end-to-end path of a connection that carries circuit-switched time sensitive traffic is referred to as 'circuit emulation' on the packet network. CES allows a network operator to seamlessly migrate network core infrastructure from circuit switched to packet switched, while preserving the legacy circuit switched end equipment. A good clock synchronization scheme is essential for the successful deployment of CES. Lack of synchronization traceability between TDM equipment interconnected over the packet network may result in frame or byte slips which can affect data integrity. Thus, the effects of transmission jitter and clock drifts must be removed at the user-to-network interface. Bit rate jitter, wander, and slip rate must be kept below the thresholds defined for the TDM service.

In this paper, we analyze the properties of a clock recovery scheme which recovers transmitter bit timing information from the packet inter-arrival times. This technique does not require

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the carrying of explicit timing information within the packets. Clock recovery schemes such as synchronous residual time stamp (SRTS) [8,9] require the underlying network to have a reference timing source and some overhead is necessary to convey timing information within packets. The transmitter encodes in the outgoing packet stream, information on the frequency difference between the source clock and the reference clock, which is generated out of the common network clock available to both the transmitter and the receiver. The receiver can recover the original source clock frequency using this frequency difference information and the same reference clock. Like the techniques described in Refs. [10–14], the clock recovery scheme analyzed here is only suited for CBR traffic carried in fixed size packets over the packet network and packet losses are assumed to be low. This clock recovery scheme was first described in Refs. [13,14] for CES over ATM networks.

In this paper, we analyze how uncorrelated and correlated delay variations in the CBR traffic stream affects the quality of the clock recovered at a receiver. We prove analytically that, for a general input process with exponentially decreasing autocorrelation functions, high correlation of the delay samples produces a large variance of the recovered clock. The paper also describes all-digital implementations of the clock recovery scheme using digitally controlled oscillators such as divide-by-N counter oscillator (DNCO) and direct digital synthesizer (DDS).

2. Clock recovery based on packet inter-arrival time averaging

When transporting TDM traffic over a packet network it is necessary to ensure that both the transmitter and receiver clocks are properly synchronized. On reception, the received data encapsulated in the packets would be loaded into a play-out buffer at full physical line rate before being clocked out bit-by-bit by the receiver's clock. Two degradation mechanisms come into play when the transmitter and receivers' clocks are not synchronized:

- If the receiver clock is offset from the transmitter or if packets arrive too early or too late from the packet network, the play-out buffer will overflow or underflow resulting in either lost bits or the need for padding bits.
- The use of an inappropriate synchronization method can result in jitter and wander of the clock associated with the TDM data outbound from the packet network. Such clock imperfections can lead to observable defects on the end-service, e.g. distortion in hi-fi acoustic services, visible imperfections such as color impairments on video services, bit errors due to alignment jitter when interworking with the plesiochronous digital hierarchy (PDH) or synchronous digital hierarchy (SDH) network or frame slips when interworking with existing PSTN and narrowband ISDN (N-ISDN) networks.

Let us consider an application of CES over packet network where no common reference clock is available at both the transmitter and the receiver. In this case, the TDM receiver has to derive an estimate of the transmitter clock from the received data stream. This is commonly done using a phase-locked loop (PLL) that slaves the receiver clock to a transmitter clock (Fig. 1). The PLL is able to process transmitted clock samples encoded within the data stream [8,9], or process data arrival patterns [10–14] to generate timing signal for the receiver. The purpose of the PLL is to estimate and compensate for the frequency drift occurring between the oscillators of the transmitter clock and the receiver clock.

One of the problems with packet networks is the variable delay introduced by the packet switches, routers and through waiting time jitter which can perturb any TDM stream traversing the network. Let us consider a constant bit rate TDM stream that is fed into a packet network and the stream is mapped into fixed size packets. The packets are passed to the physical layer at regular intervals related to the time to fill the packet payload at the service clock rate. On traversing the packet network, in the absence of packet delay variation, the fixed size packets would arrive with constant inter-arrival time. However, if each packet is subjected to a different delay

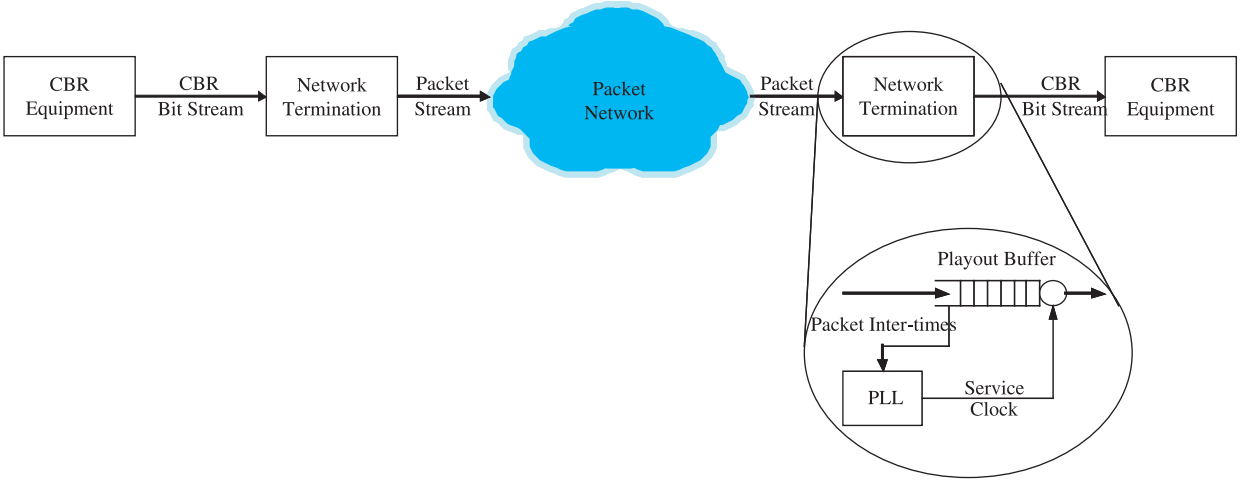

Fig. 1. Clock recovery scheme.