Int. J. Electron. Commun. (AEÜ) 67 (2013) 301–312

Contents lists available at SciVerse ScienceDirect

International Journal of Electronics and Communications (AEÜ)

journal homepage: www.elsevier.com/locate/aeue

# A novel hardware/software embedded system based on automatic censored target detection for radar systems

Ridha Djemal [a,*], Kais Belwafi [b], Walid Kaaniche [b], Saleh A. Alshebeili [c]

[a] Department of Electrical Engineering, King Saud University, Riyadh 11421, Saudi Arabia
[b] Department of Electrical Engineering, ENISo Sousse, Tunisia
[c] KACST Technology Innovation Centre in RF and Photonics (RFTONICS), King Saud University, Riyadh 11421, Saudi Arabia

ARTICLE INFO

*Article history:*
Received 7 June 2012
Accepted 11 September 2012

*Keywords:*
CFAR
FPGA
Radar
Embedded system
Co-design

ABSTRACT

This paper presents a practical design exploration for a new application related to real-time, high-resolution target detection for radar systems. In this paper, an embedded architecture that combines the hardware and software components in a single platform is experienced using a field programmable gate array FPGA-based PC-board. The detection process utilises three techniques: namely, automatic censored ordered statistics detection (ACOSD), cell averaging (CA) and ordered statistics (OS) CFAR techniques, all of which operate in parallel to increase the accuracy of the detection and to reduce the false-alarm rate for both homogeneous and non-homogeneous environments. A prototype of the embedded system detector has been implemented for homogeneous and non-homogeneous environments on Stratix IV FPGA Board. The prototype operates at 200 MHz and performs real-time target detection with an execution delay of 0.27 μs, which is less than the critical time (0.5 μs) for high-resolution detection.



## 1. Introduction

Significant studies of CFAR techniques have been carried out over the past decade to address detection problems depending on the environments in which radar systems operate. In these systems, target detection techniques require linear and nonlinear operations. The sorting technique is an example of a nonlinear operation, which consists of ranking, in ascending or descending order, the range cells according to their magnitude to yield N-ordered samples. Furthermore, the censoring technique applied to choose one ordered sample to represent the estimated noise level in the cell under test is an example of a nonlinear operation. However, some target detectors, such as the cell-averaging CFAR (CA-CFAR) and the greatest-of-selection CFAR (GO-CFAR) detector, are used to control the increase in the probability of false alarm. The architecture of the GO-CFAR detector [1] is based on linear operations by calculating the arithmetic mean of the amplitude within the window cells. All of the target detection techniques have been developed to increase the target detection probability under several environment conditions, especially those related to the region of clutter transitions and multiple-target situations.

Several CFAR processors have been proposed for use in radar systems: namely the cell averaging (CA) and the ordered-statistics (OS) processors. The CA-CFAR processor is the optimal CFAR processor in homogeneous environments. However, the assumption of a homogeneous environment is no longer valid when the number of users changes abruptly (the presence of multiple-access interference) and/or when there is fading. In such situations, the performance of the CA-CFAR processor is seriously degraded. Various classes of CFAR techniques have been proposed to enhance the robustness of this processor against non-homogeneous environments for different applications [2]. In particular, OS-based CFAR detectors have been introduced [3,4] and have proven to provide good performance in the presence of multiple-access interference (MAI). In the OS-CFAR detector, an appropriate reference cell is used to estimate the background noise power level. Even if, in homogeneous backgrounds, the OS-CFAR detector has a small additional detection loss compared with the CA-CFAR detector, it can resolve closely spaced interferences. However, the OS-CFAR detector requires a longer processing time than the CA-CFAR detector. With advances in certain technologies (DSP, ASIC, FPGA, and embedded systems), it is now possible to carry out hardware-based implementations of such complex CFAR systems with an increased capability and an acceptable time delay.

The theoretical aspect of CFAR target detection has been well developed, and a few attempts to implement CFAR processors have been reported in the literature. A parallel-pipelined hardware implementation of a CA-CFAR-based target detection system in a noisy environment using the TMS320C6203 DSP and FPGA devices has been reported [5]. The processing time achieved for

* Corresponding author. Tel.: +966 14676804.
*E-mail address:* rdjemal@ksu.edu.sa (R. Djemal).

1434-8411/$ – see front matter © 2012 Elsevier GmbH. All rights reserved.
http://dx.doi.org/10.1016/j.aeue.2012.09.001

this implementation was approximately 420 ms using 32 reference cells with 8 guarded cells. Another example of OS-CFAR implementation, using the Virtex-II-V2MB100 development kit, led to an execution time of the detection algorithms within 0.48 ms for a data set of 800 samples using only 16 reference cells, resulting in a 0.6-μs delay in cell computation [6]. These delays can be sufficient in a homogeneous environment but are not suitable for high-resolution detection, which requires less than 0.5 μs per cell. Another parallel-pipeline implementation using the CA-CFAR, GO-CFAR and SO-CFAR techniques was presented in [7]. This architecture uses 12 bits of data, and its operating frequency is 120 MHz in a XC2V250 Virtex-II FPGA device. In [8], the authors presented an FPGA-based implementation with an OS-CFAR processor using 16 bits for data processing. The proposed architecture was implemented on XCV400E-Virtex FPGA device with a maximum clock frequency of 205 MHz. A so-called ES-CFAR expert system is presented in [9] based on the sensing of the clutter environment; by means of a set of rules along with a voting scheme, this system selects the most appropriate CFAR processor to produce decisions that will outperform a single processor. This expert system is based on five separate CFAR processors: CA-CFAR, GO-CFAR, OS-CFAR, TM-CFAR and the ES-CFAR system. The latter of which is based, on the use of knowledge-based signal processing algorithms [10]. A versatile processing architecture that allows switching between six CFAR algorithms and operating parameters is presented in [11]. Other hardware implementations have been presented by Alsuwailem using other techniques related to Gaussian and Rayleigh distributions [12,13]; in these studies, the validation was performed off-line, and the real-time estimation of the performance of the system was not reported. Recently, it has been reported that a pure hardware implementation based on simulation at the RTL level of the forward ACOSD target detector of the Stratix-II development board can operate at up to 130 MHz with a delay of 0.29 μs for a log-normal distribution [14,15]. However, the proposed delay provides only an approximate delay, as no interface is defined to interconnect the detector with its environment. Therefore, the performance of the system should be updated after integrating delays related to standard interfaces and wrappers.

This work presents a new design exploration and an improvement on previous studies by integrating three algorithms such that the final decision of the target is achieved based on the results appearing in a specific display, called the target spot display, thus reducing the probability of false targets. The CA, OS and ACOSD techniques have been proposed to enhance the robustness of CFAR detectors against both homogeneous and non-homogeneous environments. Given a homogeneous background, when the reference cells contain independent and identically distributed (IID) observations governed by a Gaussian distribution, the CA-CFAR algorithm is recommended. In various non-homogeneous environments where multiple targets occur with clutter edges in the reference window, the order statistics (OS) detector is chosen, yielding good performance. Another case is also considered: the situation in which the number of interfering targets is unknown in a log-normal clutter, which occurs in many practical situations and for which the F-ACOSD algorithm is considered. The factors motivating this work are summarised as follows:

- In a homogeneous environment, it is easy to estimate the threshold adaptively with reduced computational cost using CA-based techniques.
- In a non-homogeneous environment, the OS detector features clutter with a Gaussian $P_{df}$, which results in a Rayleigh-distributed amplitude at a lower resolution. However, if we consider a high resolution with low grazing angles and a horizontal polarisation, the distribution should be log-normal.
- In the case of high resolution, low grazing angles and horizontal polarisation at high frequencies, the amplitude statistics of clutter returns deviate from a Rayleigh to a log-normal distribution.
- The adaptive threshold is based on ranked samples of reference cells to reduce cell loss and improve the detection probability of a log-normal-based distribution.

In the rest of this paper, we will consider a novel hardware/software implementation of the CA, OS and ACOSD-CFAR algorithms [15,16] for SoC implementation validated using FPFA on a PC board. The custom instruction approach will be considered to implement critical components, such as accelerators around the embedded system, including a Nios-II softcore CPU connected to the target components via the Avalon interface. All critical components will be exported as custom logic to operate as accelerators working in parallel, while the remaining non-critical parts of the CFAR processor are executed by the Nios-II softcore CPU within the same system-on-chip. The integration of the softcore CPU allows the designer to more easily perform validation and timing measurements within the FPGA with high accuracy based on internal timers. Furthermore, the co-design approach makes it easier to evaluate the performance of the CFAR processor and to modify the design partitioning accordingly.

This paper is organised as follows: Section 2 provides the theoretical foundation of the different CA, OS and ACOSD CFAR techniques. Section 3 presents the hardware/software approach applied for the CFAR processor and the details of the proposed architecture. In Section 4, a brief discussion of the performance improvements is presented, and the obtained HW/SW results are compared with those obtained for the software implemented. Finally, Section 5 presents concluding remarks and some directions for future research in the field.

## 2. CFAR Algorithms

### 2.1. CFAR basics and high-resolution requirements

A typical CFAR processor is shown in Fig. 1. The input signals are set serially in a shift register. The content of the cells, commonly called reference cells or the reference window, surrounding the cell under test $X_0$ is processed using a CFAR processor to obtain the adaptive threshold $T$. Then, the value of $X_0$ is compared with the threshold to make the decision. The cell under test $X_0$ is declared as a target if its value exceeds the threshold value $T$.

Several types of CFAR techniques based on the method used to obtain the adaptive threshold from the reference window cells have been reported in the literature [11] for different backgrounds. Of these techniques, we are interested in the CA and OS CFAR techniques in the case of homogeneous and non-homogeneous environments and in the ACOSD techniques in the case of high-resolution target detection. This requires a great computational load to be processed in real time with a limited computation delay. In this respect, the delay is fixed by the pulse width $T < 0.5$ μs, which represents a pulse width for several practical applications when clutter is viewed in the desert at high resolution and at low grazing angles ($\phi < 5^\circ$), regardless of the radar resolution [17]. Because of the complexity of the ACOSD technique, particular attention is given to the implementation of this CFAR technique, which has not yet been tested with a real architecture.

### 2.2. The CA-CFAR (distribution is exponential)

The cell-averaged (CA) CFAR technique is one of the most common CFAR detection schemes used in adaptive threshold estimation for target detection. The adaptive threshold