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Topology selection for high-precision Vernier digital-to-time converters in standard CMOS

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ABSTRACT

This paper presents two architectures that apply the Vernier delay line principle to the field of digital-to-time conversion. Both architectures are compared in terms of variability, power consumption, and area. The results show that the optimal architecture depends on the required delay resolution, on technology parameters, and on the relative importance given to power and area. If the required resolution is much smaller than the unit delay and single-shot precision is important, a topology using a matrix of delay elements provides a better power-mismatch tradeoff. If the required resolution is modest, if there is a stringent area spec, or if the focus is on linearity rather than single-shot precision, a dual delay line topology is to be preferred. The paper also derives a Pelgrom-like mismatch law for propagation delay, which can be used in the design of different types of circuits and will become more valid in future CMOS generations.

1. Introduction

Time-to-digital (TDC) and digital-to-time converters (DTC) exploit the ever increasing speed of modern CMOS transistors in order to detect or generate digital pulses with picosecond resolution. TDCs are frequently used in time-of-flight ranging applications [1–3], but can also be used in analog-to-digital converters [4] in order to replace the very limited voltage accuracy presented by modern CMOS technologies by time-domain accuracy. Similarly, DTCs can be used in two-way ranging applications, digital-to-analog converters [1], or fully digital RF transmitters [5].

Delay lines are a known way of implementing high-precision TDCs and DTCs [1,3,5,6]. However, the resolution of implementations using a single delay line is generally limited to a certain unit delay, which is usually about one inverter delay. The resolution can be further improved using techniques such as resistive interpolation [5,7], but this usually does not provide improvements of more than a factor of 2–4.

Vernier delay lines are often used in TDCs for improving the resolution [8,9] by using two delay lines with slightly different delays T_{slow} and T_{fast}. Since the resolution is now equal to $T_{res} = T_{slow} - T_{fast}$, it can be improved by orders of magnitude compared to the fastest achievable unit delay T_{fast}.

In this paper, the Vernier principle is adapted to be used in DTCs. A high-precision DTC will be implemented that can create N different delays with a resolution T_{res}. Thus it spans a total range of NT_{res}, which should be in the order of magnitude of T_{fast}. The dynamic range can then be further extended using a coarse DTC with a resolution $T_{coarse} = NT_{res}$. Such DTCs can be implemented using a single delay line and are treated extensively in literature. Therefore, this paper will only focus on the high-precision part of the DTC.

In this work, two different Vernier DTC architectures are proposed and compared based on delay mismatch, power consumption, and area. Section 2 presents the proposed architectures. In Section 3, Pelgrom's variability law is extended to propagation delay. This law is not only useful for the designs presented here but can be used for any unclocked digital circuit. The obtained Pelgrom law is used to compare both architectures in terms of mismatch in Section 4. Next, the architectures are compared in terms of power consumption in Section 5, and in terms of area usage in Section 6. An overall comparison is performed in Section 7. In Section 8, the derived theory is verified using simulations in a 40-nm CMOS technology. Finally, Section 9 concludes the paper.

2. Proposed architectures

Fig. 1a shows the first proposed architecture, which is based on two delay lines with unit delays T_{fast} and T_{slow}, respectively. Note

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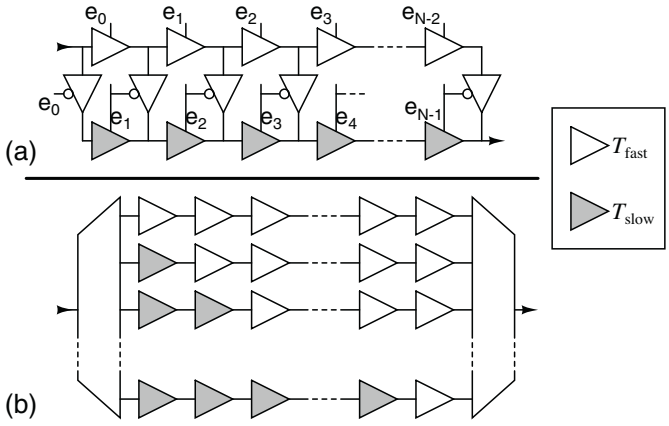

Fig. 1. Proposed architectures: (a) dual delay line architecture; and (b) matrix architecture.

that all delay elements in this architecture are tristate delay elements. The shortest delay, NT_{fast}, is achieved when $e_{N-1} = 0$ and all other e_i are equal to 1, so that the input signal only goes through fast delay elements. The longest delay is achieved when $e_0 = 0$ and all other e_i are equal to 1. In this case, the delay is equal to $T_{\text{fast}} + (N-1)T_{\text{slow}} = NT_{\text{fast}} + (N-1)T_{\text{res}}$. Thus, this block has a fixed latency of NT_{fast}, plus a delay that varies from 0 to $(N-1)T_{\text{res}}$ in steps of T_{res}. Intermediate delays are achieved by setting one e_i to 0 and the others to 1.

Fig. 1b shows the second proposed architecture, which is based on an $N \times N$ matrix of delay elements. A multiplexer (MUX) at the end selects which delay line output is used. A demultiplexer (DEMUX) is added at the input to ensure that only the delay line that is used consumes power. The top delay line produces a delay of NT_{fast}, while the bottom delay line produces a delay of $T_{\text{fast}} + (N-1)T_{\text{slow}} = NT_{\text{fast}} + (N-1)T_{\text{res}}$.

In this second architecture, T_{fast} and T_{slow} are potentially smaller than in the first one since the delays are regular delay elements (i.e. not tristate delay elements). However, if they are sized such that T_{res} is the same in both architectures, then they both provide the same delay range. The latency is different due to the different unit delays and due to the MUX and DEMUX, but this is not important in most applications.

In this work, CMOS inverters will be used for the regular delay elements, while the tristate delay elements are implemented as tristate inverters.

3. Pelgrom's law for delay

This section shows that a formula very similar to Pelgrom's mismatch law [10] is valid for the propagation delay of an inverter. This result will be used in the following section.

In [11, p. 200, eq. (5.17)–(5.18)], it is shown that the propagation delay of a CMOS inverter switching from 0 to V_{dd} or vice versa is given by

$$\tau = \ln(2) R_{\text{eq}} C_L, \tag{1}$$

where C_L is the load capacitance and R_{eq} is the equivalent resistance of the active transistor (it will be assumed here that R_{eq} is the same for the nMOS and the pMOS transistor). R_{eq} is given by

$$R_{\text{eq}} = \frac{3}{4} \frac{V_{\text{dd}}(1 - 7\lambda V_{\text{dd}}/9)}{\beta \left((V_{\text{dd}} - V_{\text{th}}) V_{\text{dsat}} - {V_{\text{dsat}}}^2/2 \right)}, \tag{2}$$

where

$$\beta = \mu C_{\text{ox}} \frac{W}{L}, \tag{3}$$

μ, C_{ox}, V_{th}, V_{dsat}, and λ are technology parameters and W and L are the transistor width and length, respectively. It should be noted that V_{dsat} and λ actually depend on L [11], but since digital circuits use only minimal-length transistors in order to achieve the lowest possible delay, they can be treated as constants here.

Pelgrom's law states that due to process variability, V_{th} and β suffer from normally distributed variations with zero mean and standard deviations $\sigma_{V_{\text{th}}}$ and σ_β, respectively. Furthermore, it says that

$$\sigma_{V_{\text{th}}} = \frac{A_{V_{\text{th}}}}{\sqrt{WL}}, \tag{4}$$

$$\frac{\sigma_\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}}, \tag{5}$$

where $A_{V_{\text{th}}}$ and A_β are technology-related constants. Assuming the distributions of V_{th} and β are uncorrelated, and that the variations are small enough so R_{eq} can be linearized with respect to V_{th} and β, the standard deviation of the propagation delay τ can be written as

$$\sigma_\tau = \sqrt{\left(\frac{\partial \tau}{\partial V_{\text{th}}} \sigma_{V_{\text{th}}} \right)^2 + \left(\frac{\partial \tau}{\partial \beta} \sigma_\beta \right)^2}. \tag{6}$$

Using (1), it follows that

$$\frac{\sigma_\tau}{\tau} = \frac{1}{R_{\text{eq}}} \sqrt{\left(\frac{\partial R_{\text{eq}}}{\partial V_{\text{th}}} \sigma_{V_{\text{th}}} \right)^2 + \left(\frac{\partial R_{\text{eq}}}{\partial \beta} \sigma_\beta \right)^2}, \tag{7}$$

which can be elaborated using (2) to

$$\frac{\sigma_\tau}{\tau} = \sqrt{\left(\frac{\sigma_{V_{\text{th}}}}{V_{\text{dd}} - V_{\text{th}} - V_{\text{dsat}}/2} \right)^2 + \left(\frac{\sigma_\beta}{\beta} \right)^2}. \tag{8}$$

Finally, substituting (4) and (5) into this equation leads to

$$\frac{\sigma_\tau}{\tau} = \frac{A_\tau}{\sqrt{WL}}, \tag{9}$$

where

$$A_\tau = \sqrt{\frac{{A_{V_{\text{th}}}}^2}{\left(V_{\text{dd}} - V_{\text{th}} - V_{\text{dsat}}/2 \right)^2} + {A_\beta}^2}. \tag{10}$$

Eq. (9) has exactly the same form as (5). It follows that delay mismatch is approximately governed by a law similar to Pelgrom's law. Due to the dependency of V_{dsat} on L, the Pelgrom constant A_τ depends on L as well, so that the law does not behave like the standard Pelgrom laws when L is changed. However, since digital circuits virtually always use minimal-length transistors, this is normally not a problem. Furthermore, since V_{dsat} is proportional to L [11], the contribution of V_{dsat} (and thus of L) in (10) becomes negligible when L becomes small. It can be shown that for L below 65 nm, the dependence on L is negligible. For example, if $L = 40$ nm, $V_{\text{dsat}}/2 \approx 15$ mV, which is much smaller than $V_{\text{dd}} - V_{\text{th}}$. This means that with decreasing minimal feature sizes, the dependence of A_τ on L becomes negligible, which turns (9) into a standard Pelgrom formula.

The law derived here allows characterizing any delay element topology by its unit delay τ when loaded with an equal delay element, and its Pelgrom constant A_τ. Since delay elements are the main building blocks in unclocked digital circuits, this makes the law relevant for all unclocked digital design.

From (9) one can conclude that σ_τ is proportional to τ, and thus to both R_{eq} and C_L. This result will be used in the next section.