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A new systematic design approach for low-power analog integrated circuits

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ABSTRACT

In this paper, a new design approach for systematic design and optimization of low-power analog integrated circuits is presented based on the proper combination of a simulation-equation based optimization algorithm using geometric programming as an optimization approach and HSPICE as a simulation and verification tool by a knowledge-based transistor sizing tool which uses physical-based gm/I_D characteristic in all regions of transistor operation to increase the accuracy in a reasonable simulation time. The proposed design methodology is successfully used for automated design and optimization of an operational amplifier with hybrid-cascode compensation using 0.18 μm CMOS technology parameters with the main purpose of minimizing the power consumption of the circuit.

1. Introduction

Due to the current rapid growth of the portable electronics market such as wireless communication systems, battery-powered consumer electronics and implantable medical electronic devices, the demand for low-power analog and mixed-signal integrated circuits is increasing. However, the continuous trend toward smaller feature sizes and higher scale of integration with lower supply voltages has increased the complexity of analog integrated circuit design. Furthermore, in contrast to the fully automated digital circuit design and due to the lack of suitable and reliable design automation toolboxes for analog integrated circuits, design of analog integrated circuits is still the most challenging and time-consuming task in the field of integrated circuit design. Several analog design automation techniques have been reported in the literature [1–17]. These methods can be categorized into two main groups, which are known as "knowledge-based" [1–3,16,17] and "optimization-based" methods [4–15]. However, optimization-based methods can itself be classified into two categories which are known as "simulation-based" [4,5] and "equation-based" optimization approaches [6–15]. However, the application of knowledge-based techniques is limited due to the requirement of having a new set of design rules which should be created by an expert analog circuit designer for every new circuit. So, the performance of such a method may fail when an expert designer does not exist. Simulation-based optimization approach uses a SPICE-like circuit simulator inside a loop of optimization and employs optimization algorithms which iteratively adjust the design variables such as transistor sizes in order to meet the constraints and desired objectives. But, the main limitation of this approach comes from the requirement of time-consuming circuit simulations for each iteration of the optimization algorithm and most of the times this method can just find the locally optimal solution not the globally optimal solution. On the other hand, Equation-based optimization algorithm evaluates the circuit performances using simplified (first or second-order estimations) circuit equations and transistor models and does not consider the higher order effects which are very important in the behavior modeling of deep-submicron transistors in the recent CMOS technologies. As a result, the obtained solution may deviate from the real solution and in some cases this approach may fail to provide even a feasible solution.

In this paper, a simulation-equation based optimization approach using geometric programming (GP) as an optimization tool and HSPICE as a circuit simulator is used to gain the benefits of both optimization approaches while avoiding their shortcomings. In contrast with previous design approaches, the proposed design algorithm uses bsim3v3 CMOS transistor model to improve the accuracy. Furthermore, the optimization approach uses the intervention of the knowledge of an expert analog designer by using a knowledge-based design procedure which is known as "physical-based gm/I_D design method" to sequentially fine-tune the optimization algorithm to find the optimum solution. This method provides the designer with a clear vision over all the transistor operation regions (weak, moderate, strong inversion) and hence a useful way for estimation of transistor dimensions. The gm/I_D method could also be very helpful especially in the low-power analog integrated circuit design, because this approach enables the designer to choose the moderate inversion region to obtain a reasonable speed-power trade-off which is the most

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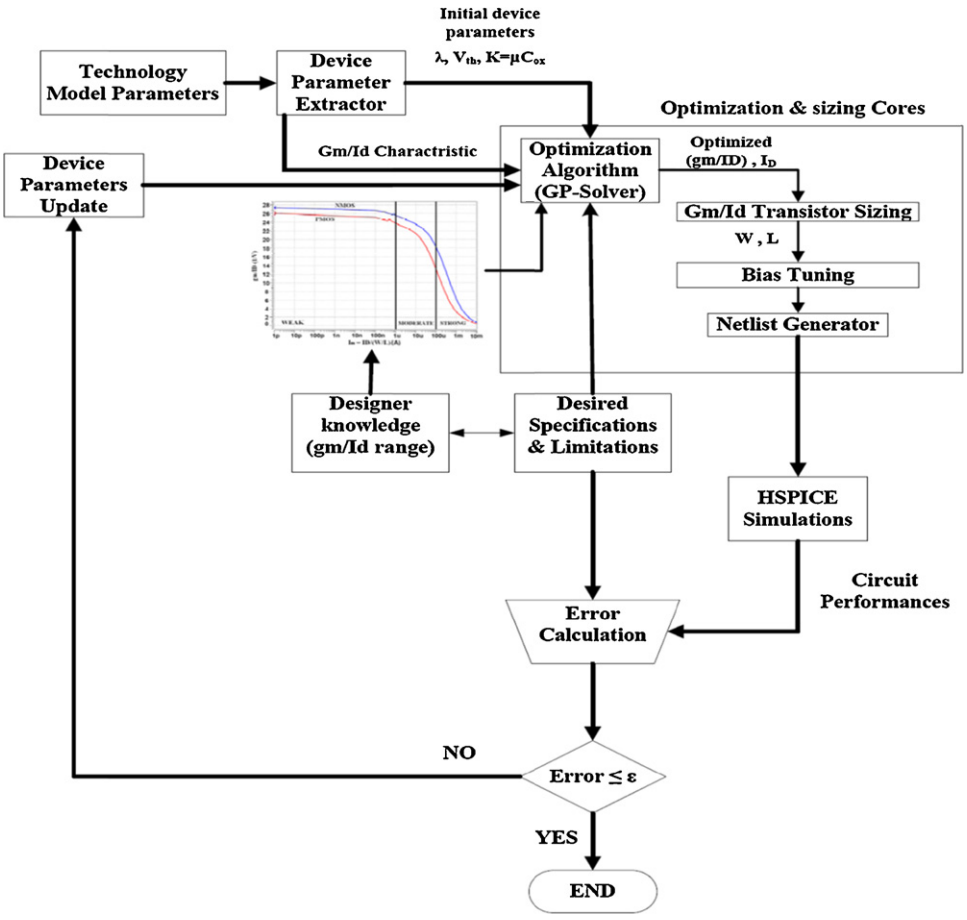

Fig. 1. Proposed design methodology.

challenging task in the low-power analog integrated circuit design [16]. This paper is organized as follows: Section 2 discusses the proposed design methodology and its main features. In Section 3, the application of the proposed design approach to the design of a low-power CMOS OPAMP is presented. In this case, the main optimization objective is to minimize the power consumption. In Section 4, simulation results of the proposed methodology are presented. Finally, the conclusion is presented in Section 5.

2. Proposed design methodology

As it is discussed before, the main design variables in the previously published literature are transistor dimensions W, L which are calculated directly from the GP solver. But, this approach fails when a sub-micron process is used because of higher order effects that appear in the sub-micron transistor behavior which impose a great amount of error to the calculations. However, this problem is solved in this paper by changing the design variables from transistor dimensions to the values of (gm/I_D) parameter and the drain current I_D for each transistor. So, the GP solver calculates the optimized values of design variables with regard to the knowledge-based constraints on the value of (gm/I_D) parameter for each transistor which is defined by the designer based on the role of each transistor in the circuit. So, when the best values for (gm/I_D) and I_D are chosen, the transistor dimensions can be easily calculated using the gm/I_D characteristic curve. Furthermore, considering the fact that most of the optimization algorithms use device equations in the strong inversion region, by using the proposed method the designer does not need to enter the complex device equations of weak and moderate inversion regions which most of the times are not in the form of convex functions and cannot be solved using geometric programming to the optimization core. Fig. 1 shows the proposed design methodology which consists of an optimization core that uses geometric programming as one of the fastest optimization methods to obtain the globally optimum solution for the design equations and gm/I_D design and sizing core which is a knowledge-based transistor sizing approach that is proposed as a physical-based low-power analog synthesis tool and cooperates with the optimization tool to properly size the transistors dimensions in the selected technology process. Fig. 2 shows the simulated gm/I_D characteristic curve for both NMOS and PMOS type transistors in 0.18 μm CMOS technology.

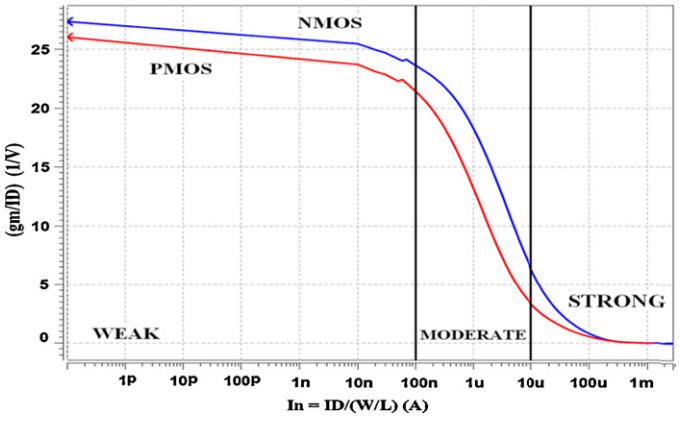

Fig. 2. Simulated gm/I_D characteristic in 0.18 μm CMOS technology.