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LETTER

Speed enhancement of a class of digital phase locked loops (DPLLs) by dynamic gain control technique

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Abstract

A dynamic gain modification algorithm of a class of digital phase locked loops (DPLLs) has been proposed. It has been shown analytically that the modified DPLL based on the proposed algorithm can be designed to have a faster transient response besides having steady-state response and frequency acquisition range same as that of a conventional DPLL. Numerical simulation results have been given to support the analytical predictions.

Keywords: Digital phase locked loop (DPLL); Transient behaviour; Stability criteria

1. Introduction

Digital phase locked loops (DPLLs) are widely used as an important building block of a modern coherent communication system. It is used in carrier regeneration, clock time recovery, FM demodulation, modem, frequency synthesizers, hard disc drive application, etc. [1–3]. From an application point of view, it is required that a DPLL should be able to reach the steady state as quickly as possible and the steady-state error parameter of the loop should be as small as practicable. Further the frequency acquisition range (FAR) of the loop should be considerably large for better acquisition and tracking performance. For conventional DPLLs, it has been observed that, for a given set of system parameters all the requirements cannot be simultaneously satisfied. When the value of the normalised loop gain would be increased from its optimum value 1, the FAR of the loop becomes large and the steady-state phase error reduces, but the transient performance of the loop degrades. As such, a few techniques have been suggested in the literature [4,5] to improve its transient response even with a large gain parameter. In this paper, we propose a new dynamic gain modification algorithm for the speed enhancement of an analog input positive zero crossing DPLL (ZC1-DPLL) even with a large loop gain condition. For this purpose, the gain of the loop digital filter (LDF) of the ZC1-DPLL has been controlled by the difference of the phase error signal of two consecutive samples of the input signal. At the transient mode of loop operation, the phase error changes at each sampling instant and thus a non-zero difference signal will be generated. This signal modifies the gain of the loop at every instance, in a direction such that the loop attains the steady state at a faster rate. As a matter of fact, the proposed modification would change the gain of the loop towards its optimum value for best transient performance. However, at the steady state the difference signal becomes zero and the effect of the modification becomes absent. Thus at the steady state, LDF become time-invariant and for this reason, the steady-state dynamics of the loop does not alters. This has been shown by deriving the stability conditions of MDPLL analytically. To compare the transient characteristics of the two structures, namely, the modified gain controlled DPLL (MDPLL) and conventional ZC1-DPLL (CDPLL), a computational method has been adopted,

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which incorporates the effect of all the possible initial phase errors within the acquisition range. The present paper is organised in the following way. Section 2 gives the structure of the system under study and formulates the system equation. In Section 3, an analysis to examine the stability of the MDPLL is reported and then a computational scheme for the comparison of the speed of convergence of MDPLL and CDPLL is given. Simulation results are given in Section 4. Finally, Section 5 offers some concluding remarks.

2. System description and system equation formulation

Fig. 1 shows the functional block diagram of a MDPLL incorporating the proposed dynamic gain modification algorithm. To study the response of the loop, we first formulate the discrete time equation of the system. Noise free and unmodulated input signal of amplitude A_0 is written in term of the angular frequency (ω_0) of the digitally controlled oscillator (DCO) as, $S(t) = A_0 \sin(\omega_0 t + \theta(t))$, where $\theta(t) = (\omega_i - \omega_0)t + \theta_0$, ω_i is the angular frequency of the input signal and θ_0 is a constant phase part. $S(t)$ is sampled at the positive zero crossing edge of the DCO. Considering the time instant of kth sample as $t(k)$, time elapsed between $(k-1)$th and kth instants is given by $T(k) = t(k) - t(k-1)$, $(k = 0, 1, ..)$. The sampled value of $S(t)$ at $t(k)$ is given by $x(k) = s(t(k))$. The sequence of the samples $x(k)$ is filtered by the LDF and the filtered version of the samples, $y(k)$ controls the period of the DCO at $(k+1)$th instant with the following algorithm [1]:

$$T(k+1) = T - y(k), \tag{1}$$

where $T(=2\pi/\omega_0)$ is the nominal period of the DCO. For a first-order CDPLL, $y(k) = G_0 x(k)$ where G_0 is the LDF gain parameter. Taking $t(0) = 0$, one can get the sampling instant $t(k)$ as

$$t(k) = kT - \sum_{0}^{k-1} y(i). \tag{2}$$

Intuitively, one can describe the purpose of the gain control algorithm in the following way. It is desired that the phase error signal should become zero or attain a constant value to bring the loop in a synchronised state. To enhance the speed of convergence, the control signal should be capable of reducing the error as quickly as possible. To achieve this, the gain of the LDF has been controlled as a function of the difference of the error signals of two consecutive instants. In the locked state this additional control signal would not be present. The variation of the LDF gain would result in adequate change in the value of $y(k)$ in the transient mode of operation. The additional error signal generated from the sampled values of the input signal at two consecutive sampling instances is given by, $x_e(k) = x(k) - x(k-1)$. $x_e(k)$ is

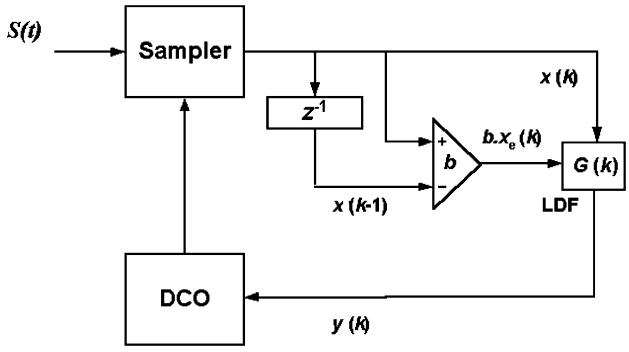

Fig. 1. Functional block diagram of a MDPLL.

used to control the gain of the LDF. Thus, the time-dependent effective gain of the LDF can be written as

$$G(k) = G_0[1 + bx_e(k)] \tag{3}$$

and $y(k)$ is taken as $G(k)x(k)$ for the modified system. Here, b is a parameter used to quantify the effect of the structure modification. We define the phase error $\phi(k)$ at the kth instant as

$$\phi(k) = \theta(k) - \omega_0 \sum_{0}^{k-1} y(i). \tag{4}$$

Using (1)–(4), one gets the phase governing equation for the MDPLL as

$$\phi(k+1) = \Lambda_0 + \phi(k) - zK_0 \sin\phi(k) \times [1 + m(\sin\phi(k) - \sin\phi(k-1))], \tag{5}$$

where $z = (\omega_i/\omega_0)$ is the normalised FAR, $K_0 = A_0\omega_0 G_0$ is the loop gain of the system, $\Lambda_0 = 2\pi(z-1)$ and $m = bA_0$ is the normalised gain modification parameter. Eq. (5) represents the system equation for CDPLL when $m = 0$.

3. Response of the system

3.1. Stability analysis of MDPLL

The stability analysis of first-order CDPLL is well documented in [6]. It is known that for stable system operation K_0 is limited as given below

$$0 < K_0 < 2 \quad \text{for } (z = 1), \tag{6a}$$

$$0 < (K_0 z)^2 - \Lambda_0^2 < 4 \quad \text{for } (z \neq 1). \tag{6b}$$

Also for an optimum transient response K_0 should be 1 for a phase step input and $(K_0 z)^2 - \Lambda_0^2 = 1$ for a frequency step input. FAR (z) can be defined as [3]

$$2\pi/(2\pi + K_0) < z < 2\pi/(2\pi - K_0). \tag{7}$$

Eq. (7) shows that, FAR is large for larger values of K_0 within the stability zone restricted by (6a) and (6b). To study