Available online at www.sciencedirect.com
ScienceDirect
Computer Communications 31 (2008) 1551–1563
computer communications
www.elsevier.com/locate/comcom

An end-to-end prototyping framework for compliant wireless LAN transceivers with smart antennas

Sébastien Roy *, Jean-François Boudreault, Louis Dupont

Radiocommunication and Signal Processing Laboratory, Department of Electrical and Computer Engineering, Laval University, Sainte-Foy, QC, Canada G1K 7P4

Available online 26 January 2008

Abstract

OFDM Wireless LANs based on the IEEE802.11 standard are complex systems in themselves. When smart antennas are used in such systems, both the MAC and the PHY layers must be redefined in order to achieve application-specific goals. As a result, the development of such systems can become impressively heavy. A complete development framework is presented here. It makes use of hardware/software co-design in order to implement all required layers to develop a wireless access point. The entire framework is targeted at an FPGA platform, providing full flexibility and processing power for the development of PHY layers.

Keywords: Field programmable gate arrays; Logic design; Integrated circuit design; Signal design; Communication system software; Communication systems; Programming environments; Software prototyping

1. Introduction

Cellular telephony has been the driving force behind wireless communications for most of the 1980s and 1990s, achieving as an industry a growth rate surpassing microcomputers. Designers today are faced with several major challenges in the continued evolution of these technologies. Many such challenges originate from an increasing pressure on the limited radio spectrum. This pressure is twofold: the number of users is growing dramatically, and the services offered and being developed are increasingly demanding in bandwidth.

Antenna arrays and associated signal processing constitute the single most promising avenue to augment both user-capacity and throughput-capacity in wireless networks. With antenna arrays at both the access point and the terminals – thus forming a multiuser MIMO system – it is possible to implement both spatial multiplexing (to augment throughput without consuming additional bandwidth) and beamforming (to support more active users and extend coverage range).

However, such systems still present many technical challenges: channel estimation and synchronization requirements are more stringent, leading to relatively complex solutions; algorithms involve vector and matrix operations and are numerically heavy; the overall design effort is much greater than with single-antenna systems. This has spurred interest in prototyping platforms and frameworks to speed up development [1–3].

The platform presented herein is specifically targeted at OFDM 802.11 networks (802.11a/g) and is fully functional at the time of this writing, although additional MAC layer functionalities are planned. Among its unique features, its software/hardware co-design architecture resides within a single platform FPGA, which interacts with a pair of secondary FPGAs fulfilling digital front-end functions. The latter interacts with custom-designed RF front-ends. Furthermore, novel algorithms have been developed for synchronization, carrier frequency offset compensation, and channel estimation within the context of multi-antenna systems [4].

* Corresponding author. Tel.: +1 418 656 2131; fax: +1 418 656 3159.
E-mail address: sebasroy@gel.ulaval.ca (S. Roy).

0140-3664/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.comcom.2008.01.016

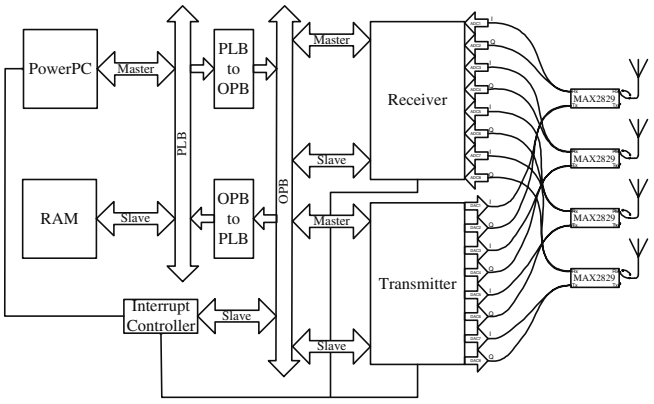

Fig. 1. System overview.

1.1. System overview

The system is built around a Xilinx Virtex II-Pro FPGA, the PHY layer being implemented as peripherals (IP cores) within the FPGA and the higher layers of the protocol (MAC, LLC, etc.) being implemented in software running on an embedded PowerPC processor within the FPGA fabric.

To support its embedded processors, the Xilinx Virtex II-Pro FPGAs include a number of dedicated peripherals and IBM CoreConnect technology, comprising the Processor Local Bus (PLB) and On-chip Peripheral Bus (OPB).

The PHY layer itself is implemented as two peripherals (receiver and transmitter) as depicted by Fig. 1. They are connected to an OPB and are interacting with the embedded PowerPC and RAM connected to the PLB bus using PLB to OPB and OPB to PLB bridges for master access in both directions.

As depicted by Fig. 2, receiver and transmitter are connected to the bus through a slave interface to provide the software with memory-mapped register access to both peripherals. A master interface is also provided to allow peripherals to interact with memory through Direct Memory Access (DMA). The pair also interact with software via interrupt lines.

At the other end, both peripherals access the RF sections through eight ADCs and eight DACs (baseband I/Q constellations on four antennas).

1.2. Platforms

1.2.1. FPGA platforms

Three FPGA platforms are used. The main processing is carried out on a *Digilent XUP-V2Pro* board, which is built around a *Virtex II-Pro XC2VP30* FPGA providing two embedded PowerPC 405 processors. Combined with 2Gbytes SDRAM as well as a serial and an ethernet link, the board offers all the resources required by the *NetBSD* operating system. A driver has been developed to support the board's Ethernet port.

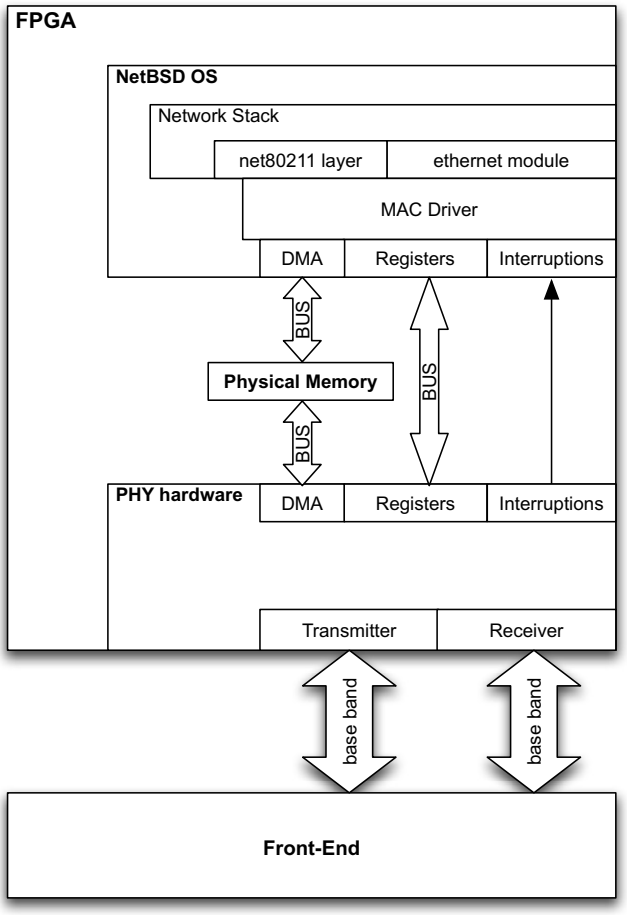

Fig. 2. Hardware/software interactions.

However, the board has no analog interface and does not offer enough general purpose I/O to interface all the ADCs/DACs required for a multiple antenna application. Furthermore, the XC2VP30 may not offer enough logic resources to implement an advanced multi-antenna transceiver in its entirety. The resource-hungry functions which are closest to the analog RF section, in effect forming a *digital front-end* (DFE), are therefore moved to other FPGAs residing in Lyrtech's VHS ADC/DAC V2 platforms. The VHS ADC provides eight analog-to-digital conversion channels to interface with up to four antennas and a Virtex II XC2V6000 FPGA. Likewise, the VHS DAC also provides eight channels for transmitting over four antennas and an identical FPGA. The VHS DAC/ADC platforms communicate with the Digilent board at the digital baseband level using a decimated sample rate, thus reducing the required throughput of the communication link, the latter being implemented using a variant of the FPDP [5] protocol.

1.2.2. RF platforms

The *Comlab Quad Dual Band RF Transceiver 6401* front-end allows baseband signals to be simultaneously transmitted and received on four RF chains in the two 802.11 fre-