Computer Networks 53 (2009) 400–417

Contents lists available at ScienceDirect

Computer Networks

journal homepage: www.elsevier.com/locate/comnet

Guaranteed real-time communication in packet-switched networks with FCFS queuing

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ARTICLE INFO

Article history:
Received 16 November 2007
Received in revised form 5 September 2008
Accepted 25 October 2008
Available online 5 November 2008

Responsible Editor: N. Akar

Keywords:
Real-time communication
Packet switching
First come first served (FCFS)

ABSTRACT

In this paper, we propose a feasibility analysis of periodic hard real-time traffic in packet-switched networks using first come first served (FCFS) queuing but no traffic shapers. Our work constitutes a framework that can be adopted for real-time analysis of switched low-cost networks like Ethernet without modification of the standard network components. Our analysis is based on a flexible network and traffic model, e.g., variable-sized frames, arbitrary deadlines and multiple switches. The correctness of our real-time analysis and the tightness of it for network components in single-switch networks are given by theoretical proofs. The performance of the end-to-end real-time analysis is evaluated by simulations. Moreover, our conceptual and experimental comparison studies between our analysis and the commonly used Network Calculus (NC) shows that our analysis can achieve better performance than NC in many cases.

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1. Introduction

Many applications, especially networked embedded real-time applications such as radar applications and control systems, require periodic hard real-time communication, meaning that every frame in the traffic stream should be 100% guaranteed to meet imposed timing requirements. Meanwhile, there is the trend of implementing embedded networks with packet-switched technologies. However, providing guarantees of timely delivery in packet-switched networks is a complicated problem because we must consider the problem of deriving the worst-case delay across multiple hops in the network.

Many approaches for solving this problem rely on adding packet scheduling, e.g., earliest deadline first (EDF), and having an admission control mechanism to verify that the specified requirements can be met [1–4]. However, packet scheduling may result in added cost and modification of the implementation, since many standard packet-switching network components only support FCFS. Consequently, standard components with FCFS queuing have been considered by many researchers. A method for calculating the worst-case packet delay in switched Ethernet with FCFS queuing has been proposed [5]. However, their method can only be applied to a limited range of applications due to assumptions on minimal-sized frames and specific traffic characteristics. Moreover, the correctness of the method has not been formally proven.

A widely accepted analytical technique, Network Calculus (NC), enables an approach for calculating the worst-case delay for FCFS queuing [6–8] and has been applied on packet-switched networks [9–14]. However, all these NC-based solutions require modification when applied to a network with standard components such as switched Ethernet, e.g., implementing traffic shapers in the source nodes [12,13] or supporting priorities to logical real-time channels [15], which significantly increase the cost and implementation complexity. Tight end-to-end delay bounds for FCFS sink-tree networks have been derived using NC [16]. However, the analysis is not generalized to

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doi:10.1016/j.comnet.2008.10.018

common network topology. In addition, NC cannot be used directly for periodic traffic, unless the periodic model is transformed into the NC traffic model. Unfortunately, such model transformation will introduce pessimism [17].

The work in this paper is motivated by (i) the need for cost-effective real-time communication solutions and (ii) the lack of real-time analysis of periodic real-time traffic for FCFS queuing. To that end, we study how to predict the worst-case delay for periodic hard real-time traffic over packet-switched networks with only FCFS queuing.

The choice of not modifying network components rises the question of how to handle burstiness and jitter in the analysis. Burstiness is the variance in traffic rate and jitter is the variation of a time metric. While it is possible to model the incoming traffic at the second hop, it is much more difficult to achieve accurate models of the traffic flows after the second hop (in networks with multiple switches) because of the difficulties in predicting aggregated jitter introduced by the previous hops. Hence, we face the challenge of predicting the traffic interference and re-characterizing the traffic arrival pattern in the intermediate network elements.

We have published a preliminary analytical framework for single-switch networks [16]. This paper extends that work with theoretical proofs and analysis for networks with multiple switches. To that end, we have the following detailed contributions.

- We propose a real-time analysis with a flexible model of the network and its traffic, allowing analysis of networks with multiple switches, variable-sized frames, arbitrary deadlines and switches with different bit-rate ports. In contrast, many existing real-time analyses in the literature are only developed for simple cases, for example, deadline being equal to period [5], a single-switch network [12,13], switches with homogeneous bit rate ports [5,12–15] or a fixed frame size [5].
- We show the correctness of our analysis by theoretical proofs. In contrast, the work on FCFS analysis in [5] does not provide any formal correctness proof of the worst-case delay calculations.
- We give theoretical proofs for the tightness of our worst-case delay analysis for network components in single-switch networks. In contrast, the delay estimations for such components are less tight in the NC analysis [11–14].
- We derive the maximum required buffer size. In contrast, some real-time analyses assume limited buffer size, which may lead to inefficient link utilization.
- We have conducted a comparison study between our analysis and NC. Our conceptual comparison shows that our analysis is tight for network components in single-switched networks, while NC is not for those cases because of the way that the traffic is modeled.
- We have developed a theory for transforming the periodic model into the rate-and-burstiness-constrained model, which has not been proposed before. Such model transformation provides the option of deriving delays for periodic traffic with NC. In this way, a better analytical scheme for any given system with periodic real-time traffic can be chosen.

Moreover, we have conducted simulations and a comparison study to evaluate the performance of our approach.

The remainder of this paper is organized as follows. Section 2 introduces the network model and the terminology. The real-time analysis for isolated network elements is presented in Section 3. The real-time analysis for a whole network is reported in Section 4. Section 5 describes a comparison study between our analysis and NC. Section 6 presents the simulation evaluation of our analysis. Finally, Section 7 concludes the paper.

2. Network model, traffic model, assumptions and relaxations

2.1. Network model

We consider a network with *Nnode* nodes and *Nswi* switches, which enables the structuring of different network topologies and different configurations, thereby supporting different types of applications. Each node and switch in the network employs FCFS queuing, that is, frames are taken from the queue in the order of arrival.

A *physical link* is a unidirectional transmission link which accepts network traffic from one network element and transfers network traffic to another network element at a constant bit rate. The bit rate of the physical link originating from source node k is denoted as $Rnode_k$ (bits/s) and the bit rate of the physical link originating from the output port p in switch s is denoted as $Rswi_{s,p}$ (bits/s).

2.2. Traffic model

A *logical real-time channel* (with index i), τ_i, is a virtual unidirectional connection from the source node, $Source_i$, to the destination node, $Dest_i$. The network maintains *Nch* multiple simultaneous logical real-time channels. As illustrated in Fig. 1, once a logical channel τ_i is established, the route, denoted by $Route_i$, is determined. $Route_i$ is a sequence of physical links each originating from a certain output port in a certain switch and can be expressed as a vector of switch/port pairs:

$$Route_i = (\langle Switch_{i,k}, Port_{i,k}\rangle), \quad k = 1, \ldots, Nr_i, \tag{1}$$

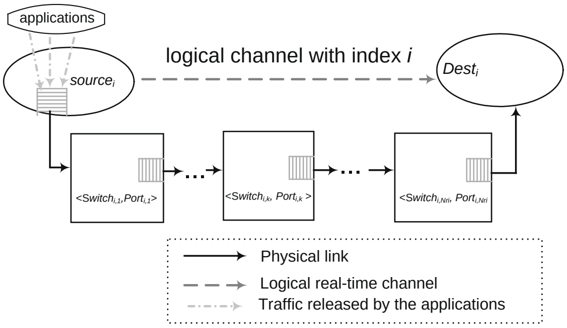

Fig. 1. Physical link and logical channel.

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