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A 25 MHz crystal less clock generator with background calibration against process and temperature variation

Wei-Bin Yang*, Ming-Hao Hong[1]

Department of Electrical Engineering, Tamkang University, 151, Yingzhuan Rd., Danshui Dist., New Taipei City, Taiwan 25137, R.O.C.

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ABSTRACT

This paper presents a crystal-less clock generator using an automatic process and temperature variation calibration technique. The crystal-less clock generator comprises a voltage-controlled oscillator (VCO), differential-input-single-output (DISO) circuit, and frequency-to-voltage converter (FVC). The VCO was developed using a four-stage differential ring oscillator to generate an output frequency of 25 MHz. The DISO circuit ensures a full-swing output voltage swing of the clock generator and a 50% duty cycle. The output clock is integrated by the FVC circuit to generate an analog voltage signal to control the VCO's oscillation frequencies. The FVC can compensate and calibrate the VCO to provide a stable output frequency through the closed-loop system. The chip was fabricated using a 0.18 μm standard CMOS process with a 0.9 V supply voltage. The measured temperature coefficient was 513 ppm/°C in the temperature range of −40°C to 125°C at a 25-MHz output frequency.

1. Introduction

The reference clock generator is a crucial component of digital circuits. The quartz crystal oscillator is the most common clock reference; it provides stability when there are variations in the process, temperature, and supply voltage. However, the oscillator increases the area and cost of the clock generator system. Therefore, investigations of on-chip crystal-less clock generator references are useful, especially for minimizing the area and cost of the devices in which they are used. The types of oscillators include inductor–capacitor (LC), resistor–capacitor (RC), and ring oscillators. Among them, LC oscillators consume the most power and provide a frequency accuracy on the order of parts per million. RC relaxation oscillators provide frequency stability; however, they typically require external resistors, which leads to an increased chip area. A complementary metal-oxide semiconductor (CMOS) ring oscillator can achieve low frequency variation without any external components. Moreover, CMOS ring oscillators are more effective for realizing a moderate-accuracy frequency reference [1].

As shown in Fig. 1, the performances of oscillator and buffer circuits will be affected by variations in process and temperature. To achieve stable oscillator output frequency in the presence of process and temperature variations, the immunity against process and temperature variations has become a key point of consideration in the design of oscillators. Over the past few decades, miscellaneous methods such as those involving switched-capacitor circuits, cascaded time-to-voltage conversion, integration and holding, successive approximation, and counter-based circuits have been presented for implementing frequency-to-voltage converters (FVCs) [2,3]. The design of a frequency-locked loop (FLL) is similar to that of a

* Corresponding author. Fax: 866-2-26209814.
E-mail addresses: robin@mail.tku.edu.tw (W.-B. Yang), accasd85259@gmail.com (M.-H. Hong).
[1] Fax: 866 2 26209814.

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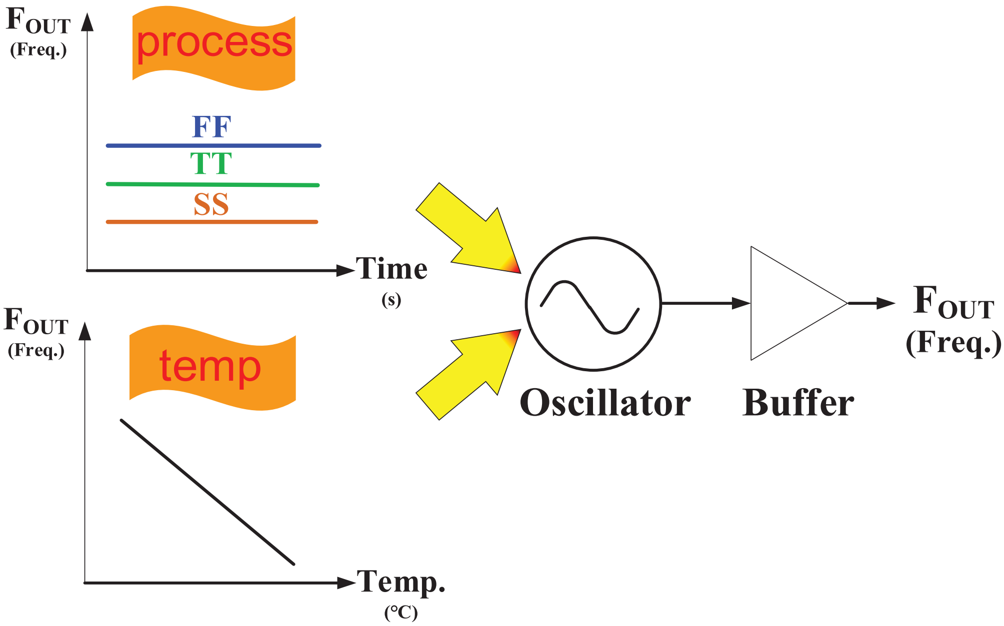

Fig. 1. Oscillator with the immunity of process and temperature variations.

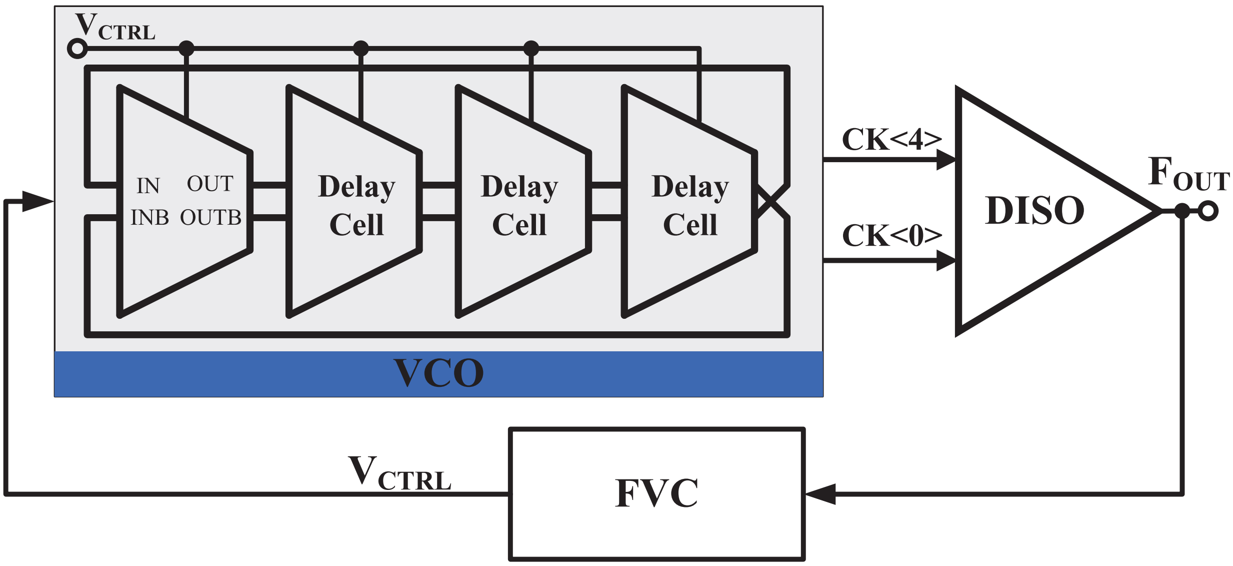

Fig. 2. The architecture of the proposed crystal-less clock generator.

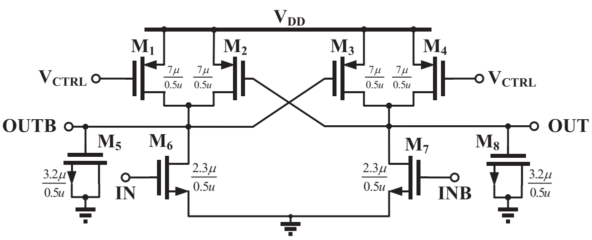

Fig. 3. The circuit architecture of delay cell.