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Hierarchical approach for hybrid wireless Network-on-chip in many-core era ☆

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ABSTRACT

Due to high latency and high power consumption in long hops between operational cores of Network-on-Chips (NoCs), the performance of such architectures has been limited. Billions of transistors available on a single chip present opportunities for new levels of computing capability. In order to fill the gap between computing requirements and efficient communications, a new technology called Wireless NoC has been emerged. Employing wireless communication links between cores, wireless NoC has reasonably increased the performance of NoC. However, wireless transceivers along with associated antenna impose considerable area and power overheads in wireless NoCs. Thus, in this paper, we introduce a hybrid wireless NoC called Hierarchical Wireless-based Architecture (HiWA) to use the wireless resources optimally. In the proposed approach the network is divided into subnets where intra-subnet nodes communicate through wire links while inter-subnet communications are handled almost by single-hop wireless links. Simulation results show that HiWA efficiently reduces power consumption by 39% in comparison with a traditional wireless NoC, called WiNoC, while still achieves 16% lower packet latency than conventional NoC.

1. Introduction

Electronic industry is changing in so swift a fashion which is, of course, the result of the permanent demand for innovation and technological advancement. Under these circumstances, manufacturers of electronic devices tend to enrich their products as much as possible; therefore, according to Moore's law, these devices are getting more and more complex. Today electronic devices require small, low-power and very fast chips to work with advanced applications. Many believe that emerging of System-on-Chip (SoC) has been an effective solution for advancement of the industry in the form of Moore's law [1,2]. As the number of cores integrated into a SoC increase the role played by the communication system becomes more and more important [3]. According to [4,5] there are two major limitations in SoC. The first limitation is the latency of long wires to connect Processor Elements (PEs) which by the decrease of technology scale, is changed into a bottleneck. The second limitation is integration of PEs with different standards and various producers on a single chip (i.e. Heterogeneous Computing). Each of these cores has its specific needs and limitations which has caused some problems for designing SoC.

The method of designing based on information which is presented as a solution for the existing challenges in designing SoC [1,4,6] has a key feature according to which, more efficient and at the same time simpler systems are tried to be provided. This

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key feature includes separating information from communication. Network-on-Chip (NoC) is a very compressed system based on network technology in which PEs are connected to each other according to a communication infrastructure consisted of a switch, router and communication links called Interconnection Network. According to [7], despite the fact that NoC has a lot of advantages because of the presence of long wires in two-sided metal interconnects, it suffers from high latency and high power consumption.

At this juncture, by way of extremely high energy costs, single-core high-frequency processors are less considered and processors manufacturers are moving toward designing multi and many-core chips. Therefore, alternative technologies such as Wireless Network-on-Chip [8,9], 3D Network-on-Chip [10] and Photonic Network-on-Chip [11] were introduced. In this paper, a hybrid wireless network-on-chip architecture called Hierarchical Wireless-based Architecture (HiWA) along with performance evaluation parameters is introduced. HiWA is based on a 2D mesh that is divided into square subnets. Then, in each subnet if necessary one of the Conventional Routers (CRs) is replaced by a Wireless Router (WR) which has wireless connections with WRs in neighbors' subnets. Moreover, A WR placement algorithm as well as a routing algorithm is proposed for HiWA. In addition, reducing number of WRs to obtain a trade-off between latency and power consumption has been targeted. The rest of the paper is organized as follows. Section 2 review backgrounds and related works. The HiWA architecture is proposed in Section 3. Section 4 evaluates HiWA based on performance parameters. Finally, some conclusions are given in Section 5.

2. Backgrounds and related works

Recent progresses in silicon integrated circuit technology have permitted the integration of tiny transceivers antennas on a single chip, which results in introducing Wireless Network-on-Chip (Wireless NoC). In [12] transceivers for 60 GHz inter and intra-chip communications are designed. In [13] on-chip wireless transceivers are utilized to assist the progress of fast pre-bonding wafer testing enabled by direct accesses to components under test within the ICs. A low Terahertz (324 GHz) frequency generator is fulfilled in 90 nm CMOS [14]. Moreover, a signal source operating near 410 GHz that is fabricated using low-leakage transistors in a 6 M 45 nm digital CMOS technology is reported [15]. Based on these techniques, the output power level of the on-chip millimeter-wave generator can be as high as −1.4 dBm in the 32 nm CMOS process, which is large enough for on-chip short distance communication [16]. Following the rule of thumb in RF design, the highest available bandwidth is 10% of the carrier frequency. According to this experimental estimation, up to 16 channels can be available for wireless NoC in the range of 100–500 GHz. With recent developments of millimeter-wave circuits, bandwidths of hundred GHz will be reachable in near future. In addition to the bandwidth, wireless NoC requires low-power on-chip wireless transceivers. Silicon Mach-Zehnder electro-optic modulator at data rates up to 10 Gb/s with low RF power consumption of only 5 pJ/bit [17] is commercially available.

Beyond traditional wired interconnect solutions, different emerging approaches including 3D Network-on-Chip and Photonic Network-on-Chip were proposed [10,11]. In addition, the design of a wireless NoC based on CMOS UWB technology is introduced [18]. The antennas used in [18] achieve a transmission range of 1mm; therefore, for a typically die area of 20 mm×20 mm, this architecture requires multi-hop communication. Additionally, a broad survey regarding different wireless NoC architectures and their design doctrines is given in [19]. Furthermore, using miniaturized on-chip antennas as an enabling technology, a hybrid wireless NoC (WiNoC) is designed [7]. Complex design steps used in WiNoC require high hardware overhead to implement in micro-architecture level. Graphene or Carbon Nano-Tube (CNT) based on-chip antennas are anticipated to support high bandwidth wireless communication channels [20,21]. Since integration of CNT antennas with standard CMOS technology faces serious challenges, utilizing mm-wave CMOS transceivers running in the sub-THz frequency ranges seems to be a more feasible solution. Thus, in [22] mm-wave on-chip wireless antennas for both inter and intra-chip communications are modeled and evaluated.

In this paper, a hierarchical wireless network-on-chip architecture is introduced. Although several aspects of the proposed architecture are addressed in the paper, HiWA is a flexible platform that different placement and routing algorithms can be applied to it without changing the architectural structure. With optimal placement of WRs a trade-off between latency and power consumption parameters is obtained. The trade-off criteria are easily changeable according to the application where HiWA will be used.

3. Proposed architecture

3.1. Topology

The backbone of the proposed Hierarchical Wireless-based Architecture, HiWA, is based on 2D mesh NoC. The topology is shaped in such a way that first 2D mesh is divided into square subnets; then, in each subnet if necessary one of Conventional Routers (CRs) is replaced by a Wireless Router (WR) which has wireless links with WRs in neighbors' subnets. WRs are capable of performing both wired and wireless communication.

3.2. Addressing

Addressing method in HiWA is formed of X_{subnet}, Y_{subnet}, X_{local}, and Y_{local} in which the first two fields indicate the location of subnet and the next two fields determine the place of local node (router) in the subnet. Separating local and subnet address fields results in a simple design of hierarchical systems. Besides, it decreases hardware complexity of routers.