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A design of low swing and multi threshold voltage based low power 12T SRAM cell ☆

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ABSTRACT

This paper focuses on the design of a novel low power twelve transistor static random access memory (12T SRAM) cell. In the proposed structure two voltage sources are used, one connected with the bit line and the other one connected with the bitbar line in order to reduce the swing voltage at the output nodes of the bit and the bitbar lines, respectively. Reduction in swing voltage reduces the dynamic power dissipation when the SRAM cell is in working mode. Low threshold voltage (LVT) transmission gate (TG) and two high threshold voltage (HVT) sleep transistors are used for applying the charge recycling technique. The charge recycling technique reduces leakage current when the transistors change its state from sleep to active (OFF to ON condition) and active to sleep (ON to OFF condition) modes. Reduction in leakage current causes the reduction in static power dissipation. Stability of the proposed SRAM has also improved due to the reduction in swing voltage. Simulation results of power dissipation, access time, current leakage, stability and power delay product of the proposed SRAM cell have been determined and compared with those of some other existing models of SRAM cell. Simulation has been done in 45 nm CMOS environment. Microwind 3.1 is used for schematic design and layout design purpose.

1. Introduction

The demand of battery operated high speed portable devices like notebook, laptop computers, personal digital assistants, cellular phones, etc. increase day by day. High speed portable devices require primary memory that responds faster. For that purpose, static random access memory (SRAM) is used, which is faster and refreshing is not needed again and again. Dynamic power dissipation and leakage current are the main issues of high speed SRAM cells because this unwanted power dissipation reduces the battery backup life of portable devices. So it is required to have a SRAM cell design, having both low static and dynamic power dissipations.

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Supply voltage is scaled to maintain the power consumption within limit. However, scaling of supply voltage is limited by the high performance requirement. Hence, the scaling of supply voltage only may not be sufficient to maintain the power density within limit, which is required for power sensitive applications. Circuit techniques and system level techniques are also required along with supply voltage scaling to achieve low power designs [1].

Aggressive scaling of the devices not only increases the subthreshold leakage but also has other negative impacts such as increased drain induced barrier lowering (DIBL), threshold voltage (*V*th) roll off, reduced on current to off current ratio, and increased source to drain resistance [2]. *V*th roll off increases the dependence of *V*th on the channel length. A small variation in channel length might result in large threshold voltage variation, which makes device characteristics unpredictable. To avoid these short channel effects, oxide thickness scaling and higher and non uniform doping need to be incorporated [3] as the devices are scaled. The low oxide thickness gives rise to high electric field, resulting in considerable direct tunnelling current [4]. Higher doping results in high electric field across the reverse biased p–n junctions (source-substrate or drain-substrate) which cause significant band to band tunnelling (BTBT) of electrons from the valence band of the p region to the conduction band of the n region. Peak halo doping (P+) is restricted such that the BTBT component is maintained reasonably small compared to the other leakage components.

In another technique [5], a low area overhead adaptive body bias (ABB) circuit is proposed to compensate for aging and process variations to improve the SRAM reliability and yield. The proposed ABB circuit consists of a threshold voltage sensing circuit and an on chip analog controller for power reduction. A multi threshold complementary metal oxide semiconductor (MTCMOS) technology provides low leakage and high performance operation by utilizing high speed, low threshold voltage (LVT) transistors during active mode and low leakage, high threshold voltage (HVT) transistors during sleep mode, which reduces the static power dissipation of the SRAM circuit [6,7].

In [8], a technique to reduce both the active and standby powers, especially at room temperature, has been discussed. A bit line power calculator is used to adaptively set the cell supply voltage in the active mode. A digitally controllable retention circuit regulates in the standby mode with small control power. These circuits are implemented in a dual power supply SRAM in 28 nm CMOS technology. In another approach a 5T SRAM cell is proposed with fast performance, high density and low power consumption [9]. The proposed complementary metal oxide semiconductor (CMOS) SRAM cell consumes less power and has less read and write times. The cell is based on the single ended memory storage principle. This scheme is based on the static power reduction. In [10], a symmetrical topology based SRAM cell has been proposed for higher stability. In that two transistors isolate the cell storage nodes from the read operation path to maintain the data stability of the cell. This topology improves the data stability.

A low power multiport SRAM with cross point write word lines shared write bit lines and shared write row access transistors approach has been shown in [11]. The design has one write, one read and two write, two read multi port SRAMs for register file applications in nanoscale CMOS technology. The cell features a cross point write word line structure to mitigate write half select disturb and improves the static noise margin (SNM). The write bit lines (WBLs) and write row access transistors are shared with adjacent bit cells to reduce the cell transistor count and area. The scheme halves the number of WBL, thus reducing WBL leakage and power consumption. In addition, column based virtual ground control is employed for the read stack to reduce the read power consumption. In [12], SRAM cell achieves low power dissipation due to its series connected drivers driven by bit lines and read buffers which offer stack effect. This approach is based on static power dissipation.

In this present work a novel low power 12T SRAM cell is proposed. A charge recycling technique is used to minimize the leakage currents and static power dissipation during the mode transitions. Two voltage sources are used at the output nodes to reduce the swing voltages, resulting in reduction of dynamic power dissipation during switching activity. The different performance parameters have been determined for the proposed SRAM cell and compared with those of the other existing SRAM cells.

The paper is organized as follows: Section 2 discusses about some existing SRAM cells, Section 3 describes circuit design and working principle of the proposed novel 12T SRAM cell. Section 4 describes the detailed analysis of the characteristics of the proposed cell and comparison with other existing SRAM cells and finally, Section 5 concludes the paper.

2. Existing SRAM cells

Fig. 1(a) shows the circuit diagram of a conventional SRAM cell [13]. Before the read operation begins, the bit line (*BL*) and bitbar line ($\overline{BL}$) are precharged to as high as supply voltage V_{dd}. When the word line (WL) is selected, the access transistors are turned on. This will cause a current to flow from supply voltage (V_{dd}) through the pull up transistor TP1 of the node storing "1". On the other side, current will flow from the precharged bitbar line to ground, thus discharging bitbar line. Thus, a differential voltage develops between the *BL* and $\overline{BL}$. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output.

The 6T single ended SRAM cell [14] is shown in Fig. 1(b). This cell design uses two assist transistors, one for the memory read access (MRA) purpose and the other for the memory write access (MWA) purpose. During write operation, with the BL precharged to required value, write word line (WWL) is held high and MWA is held OFF so as to weaken the cross coupled inverter and hence, get a successful write. During read, read word line (RWL) is held high and read occurs through M6 and MRA depending upon the value stored at the node QB.